Edit Date: (5/27/01)

IP2022 Datasheet Errata

The IP2022 datasheet and User's Manual have been updated to reflect enhancements planned for the upcoming IP2022 silicon Rev 2.0. Ubicom is currently sampling Rev 1.0 silicon.

The revisions of the datasheets and User's Manual dated January 22, 2001 and prior reflected Rev 1.0 silicon. Several new sections have been added to the datasheet to reflect Rev. 2.0 silicon. The release date for the updated documentation is May 27, 2001. The updates include:

Item 1
Type of Change: Design New Block (LFSR)
Data Sheet Section: 5.9.

Description:

Added four Linear Feedback Shift register (LFSR) and all of the sub-sections. LFSR blocks are used to perform CRC and other operations. LFSR0 and LFSR2 are dedicated for SerDes1 and LFSR1 and LFSR3 support SerDes2.

Item 2
Type of Change: Design New block(Ext. Memory)
Data Sheet Section: 5.11.

Description:

Added external memory interface and all of the sub-sections. RB4:7 and RC7:0 and RD7:0 are used for the interface.

Item 3
Type of Change: Design New block (Squelch Circuit)
Data Sheet Section: 5.6.

Description:

Squelch function has been added to RG4, RG5, RG6, RG7 pins. Use CMPCFG bit 4 to select the Squelch function. This circuitry has been added to facilitate Ethernet compliance testing.

Item 4
Type of Change: SerDes Enhancement
Data Sheet Section: 5.6.

Description:

SerDes section has been updated for improved functionality. I^2C function of the SerDes is removed and GPSI is added. In addtiona, added a register bit to select MSB or LSB first, for all SerDes protocols. GPSI uses LSB first. Default (on reset) = 0, which selects LSB first. Also, included support for reversed polarity on differential inputs for Ethernet application.

Item 5
Type of Change: Assembler
Data Sheet Section: Table 4-4

Description:

Because of a change in the assembler, the "." used in the operand field for bit operation is

clrb fr,bit ("." is now replaced by ",")
sb fr,bit
setb fr,bit
snb fr,bit

Item 6
Type of Change: New Spec
Data Sheet Section: Tables 4-9, 4-10

Description:

These tables reflects the new flash speed of 30 MHz. previously, it was 40 MHz.

Item 7
Type of Change: New Instruction
Data Sheet Section: Table 4-7

Description:

New **ireadi** and **iwritei** instructions have been added to read and write to the External Program memory and increment. Also, **iread** is now non-blocking if reading Flash from Shadow, or PRAM from Flash.

Item 8
Type of Change: New Bit Definition
Data Sheet Section: 3.8.3

Description:

New TRIM0 Register Bit definition. Watchdog Timer trim bits are removed and Squelch trim bits are added.

Item 9
Type of Change: Misc. Updates

Description:

Section 1.1: Updated Key Features. Key features now reflect the new features being designed into the Rev. 2.0 silicon.

Table 2-1: Updated Signal Description because of new blocks.
Figure 3-1: Updated Block Diagram reflects LFSR and External Memory Interface block.

Section 3.9: Updated Special-Purpose Register Map.
The Map now includes all the control registers for the LFSR and External Memory interface block.

Sections 8.1, 8.2, 8.3: Updated Electrical Characteristics with additional data.