IP2022 Internet Processor™

Features and Performance Optimized for Network Connectivity

1.0 PRODUCT OVERVIEW

1.1 Introduction

The Ubicom IP2022 Internet Processor™ combines support for communication physical layer, Internet protocol stack, device-specific application and device-specific peripheral software modules in a single chip, and is reconfigurable over the Internet. It can be programmed, and reprogrammed, using pre-built software modules and configuration tools to create true single-chip solutions for a wide range of device-to-device and device-to-human communication applications. Fabricated in an advanced 0.25-micron process, its RISC-based deterministic architecture provides high-speed computation, flexible I/O control, efficient data manipulation, in-system programming, and in-system debugging. A hardware full-duplex serializer/deserializer (SerDes) function gives the IP2022 the ability to directly connect to a variety of common network interfaces. This function provides the ability to implement on-chip 10BaseT Ethernet (MAC and PHY), USB, and a variety of other fast serial protocols. The inclusion of two SerDes units facilitate translation from one format to another, allowing the IP2022 to be used as a protocol converter. The 100 MHz operating frequency, with most instructions executing in a single cycle, delivers the throughput needed for emerging network connectivity applications, and a flash-based program memory allows both in-system and on-the-fly reprogramming. The IP2022 implements peripheral, communications and control functions as software modules (ipModules™), replacing traditional hardware for maximum system design flexibility. This approach allows rapid, inexpensive product design and, when needed, quick and easy reconfiguration to accommodate changes in market needs or industry standards.

On-chip dedicated hardware also includes a PLL, an 8-channel 10-bit ADC, general-purpose timers, single-cycle multiply instruction, analog comparator, user-selectable multi-level brown-out detector, watchdog timer, low-power support, multi-source wakeup capability, user-selectable clock modes, high-current outputs, and 52 general-purpose I/O pins.

A TCP/IP network protocol stack is available, and a variety of additional software that is necessary to form a complete end-to-end connectivity solution is being developed. Tools for developing with and using the IP2022, including the complete Red Hat GNUPro tools, are available from leading suppliers.

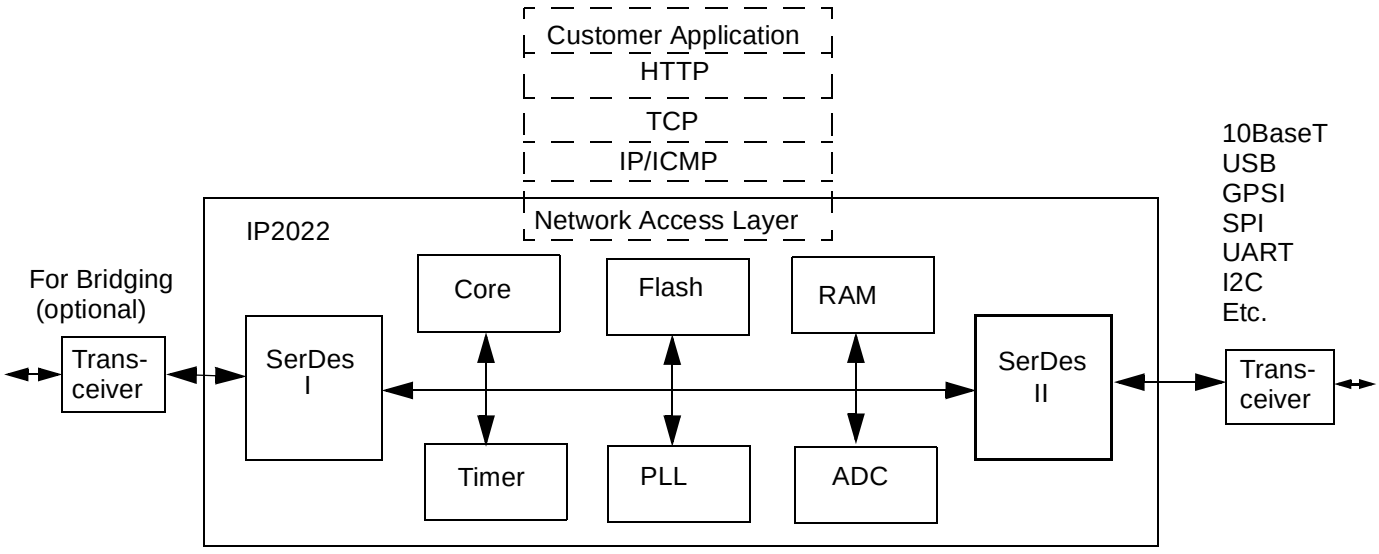

Figure 1-1. IP2022 Block Diagram

1.2 Key Features

CPU Features

- RISC engine core with DC to 100 MHz operation
- 10 ns instruction cycle
- Compact single-word (16-bit) instruction set
- Single-cycle instruction execution on most instructions
- 1 instruction per clock (3 clocks per branch)
- 16-bit instructions
- Sixteen-level hardware stack for high-performance subroutine linkage
- 8 × 8 signed/unsigned single-cycle multiply
- Pointers and Stack operation optimized for C compiler

On-chip Memory

- 64 Kbyte (32kx16) program flash memory
- 16 Kbyte (8kx16) program/data RAM
- 4 Kbyte Data RAM
- Self-programming with built-in charge pump: instructions to read, write, and erase

Fast and Deterministic Program Execution and Interrupt Response

- Predictable execution rate for hard real-time applications
- Fast and deterministic 3-cycle internal interrupt response
  - 30 ns internal interrupt response at 100 MHz including context save
- Hardware save/restore of register context (PC, W, STATUS, MULH, SPDREG, IPH, IPL, DPH, DPL, SPH, SPL, ADDRH, ADDRL, DATAH, DATAL)

Multiple Networking Protocols and Physical Layer Support Hardware

- Two full-duplex serializer/deserializer (SerDes) channels for 10BaseT (MAC/PHY), USB, and other fast serial protocol support
  - Embedded connectivity nodes
  - Two channels for protocol bridging
  - I^2C, UART, SPI, Microwire/PLUS

General-Purpose Hardware Peripherals

- Two 16-bit timers with 8-bit prescalers supporting:
  - Timer mode
  - PWM mode
  - Capture/Compare mode
- Slave parallel/host interface, 8/16-bit selectable for use as a communications co-processor
- One 8-bit timer with programmable 15-bit prescaler
- One 8-bit real-time clock/counter with programmable 8-bit prescaler and 32 KHz crystal input
- Watchdog timer with postscaler
- On-chip PLL clock multiplier with pre- and post-divider
  - 4 MHz input produces 100 MHz internal operating frequency
- 10-bit, 8-channel ADC with 1/2 LSB accuracy
- Analog comparator with hysteresis enable/disable
- Brown-out minimum supply voltage detector
- External interrupt inputs on 8 pins (Port B)

Sophisticated Power and Frequency/Clock Management Support

- Operating voltage of 2.3V to 2.7V
- Switching the system clock frequencies between different clock sources
- Changing the core clock using a selectable divider
- Shutting down the PLL and/or the OSC input
- Controlling the speed of the Core by SPEED instruction
- Power-On-Reset (POR) logic

Flexible I/O

- 52 I/O Pins
- 3.3V drive, 5V-tolerant inputs
- Symmetrical output drive
- Port A pins capable of sourcing/sinking 24 mA
- Selectable I/O operation synchronous to the CPU core clock

Programming and Debugging Support

- Updatable application program
  - Run-time self programming
- On-chip in-system programming support with SPI interface
- On-chip in-system debugging support logic with dedicated SPI interface
  - Debugging at full IP2022 operating speed
- Programming at device supply voltage level
- Real-time emulation, program debugging, and integrated software development environment offered by leading third-party tool vendors

Pre-Built Software Modules

- Selection of physical interfaces
  - 10Base-T Ethernet
  - USB
  - UART
  - I^2C
  - SPI
  - Parallel slave
- Complete TCP/IP stack

Software Support

- Red Hat GNUPro tools
  - GCC ANSI C compiler and assembler, linker, utilities, GNU debugger, and IDE
- Nohau in-circuit debugger
  - Seehau Interface
  - USB-based debug hardware
  - Assembler
- Library of off-the-shelf ipModules (Ethernet, serial interfaces, USB interface, etc.)
- Evaluation kits for Internet and communication-intensive applications

1.3 Architecture

1.3.1 CPU

The IP2022 implements an enhanced Harvard architecture with two separate memories that have independent address and data buses, a 16-bit program memory, and an 8-bit dual-port data memory. This allows instruction fetch and data operations to occur in parallel. The advantage of this architecture is that instruction fetch and memory transfers can be overlapped by a multistage pipeline, so that the next instruction can be fetched from program memory while the current instruction is executed with data from the data memory.

Ubicom has developed a revolutionary RISC-based architecture that is deterministic, jitter free, and completely reprogrammable.

The IP2022 implements a four-stage pipeline (fetch, decode, execute, and write back). At the maximum operating frequency of 100 MHz, instructions are executed at the rate of one per 10 ns clock cycle.

1.3.2 Serializer/Deserializers

One of the key elements in optimizing the IP2022 for device-to-device and device-to-human communication is the inclusion of on-chip serializer/deserializers. This hardware decodes data and lets it be translated from one format to another, allowing the IP2022 to be used as a protocol converter in bridge and gateway applications.

There are two serializer/deserializer units in the IP2022 that support a variety of protocols, including SPI, I^2C, UART, USB, and 10Base-T Ethernet. By performing data serialization and deserialization in hardware, the CPU bandwidth needed to support serial communications is greatly reduced, especially at high baud rates. Providing two units allows easy implementation of protocol conversion or bridging functions, such as a USB-to-I^2C bridge.

1.3.3 Low-Power Support

Particular attention has been paid to minimizing power consumption. For example, an on-chip PLL allows use of a lower-frequency external source (e.g., an inexpensive 4 MHz crystal oscillator can be used to produce a 100 MHz internal operating frequency), which reduces both power consumption and EMI. In addition, software can change the execution speed of the CPU to reduce power consumption, and a mechanism is provided for automatically changing the speed on entry and return from an interrupt service routine. The SPEED instruction specifies power-saving modes that include a clock divisor between 1 and 128. This divisor only affects the clock to the CPU core, not the timers. The SPEED instruction also specifies the clock source (OSC1 clock, RTCLK oscillator, or PLL clock multiplier), and whether to disable the OSC1 clock oscillator or the PLL. The SPEED instruction executes using the current clock divisor.

1.3.4 Memory

The IP2022 CPU executes from a 32K × 16 flash program memory and an 8K × 16 RAM program/data memory. The instruction RAM can alternative be used for data storage. In addition, the ability to write into the program flash memory, allows flexible non-volatile RAM implementation. The maximum execution rate is 40 MIPS from flash and 100 MIPS from RAM. Speed-critical routines can be copied from the flash memory to the RAM for faster execution. The IP2022 has a mechanism for in-system programming of its flash and RAM program memories through a four-wire SPI interface, and software has the ability to reprogram the program memories at run time. This allows the functionality of a device to be changed in the field over the Internet.

1.3.5 Instruction set Architecture

The IP2022 instruction set, using 16-bit words, implements a rich set of arithmetic and logical operations, including signed and unsigned 8-bit × 8-bit integer multiply with a 16-bit product.

1.3.6 The ipModule Concept

The ipModule concept enables the “software system on a chip” approach. An ipModule is a software implementation of an interface, protocol or other function that replaces traditional hardware. This takes advantage of the Ubicom architecture’s high performance and deterministic nature to produce the same results as hardware, but with much greater system design flexibility. Having functionality implemented as pre-built software modules allows the IP2022 to be programmed and reprogrammed at any time in the design and manufacturing cycle, and even in the field over the Internet.

The speed and flexibility of the Ubicom architecture, together with the availability of Internet connectivity software modules, simultaneously address a wide range of engineering and product development concerns. They decrease the product development cycle dramatically, shortening time to production to as little as a few weeks.

Ubicom’s timesaving ipModules give system designers a choice of ready-made solutions, or a head start on developing their own peripherals. With ipModules handling established functions, design engineers can concentrate on adding value to other areas of the application.

Overall, the ipModule concept provides such benefits as simpler hardware architecture, reduced component count, fast time to market, increased flexibility in design, application customization and overall system cost reduction.

Some examples of ipModules are:

- Ethernet and USB network interfaces
- Communication interfaces such as I^2C™, Microwire™, SPI, and UART
- Internet connectivity protocols, such as UDP, TCP/IP, ARP, DHCP, HTTP, SMTP, and POP3

1.3.7 Programming and Debugging Support

The IP2022 is supported by leading third-party tool vendors. On-chip in-system debug capabilities allow these tools to provide an integrated software development environment that includes editor, assembler, debugger, simulator, and programmer tools. For example, the complete Red Hat GNUPro tools, including C compiler, assembler, linker, utilities and GNU debugger, supports the IP2022. Likewise, the Seehau interface, high-end debugger, assembler and USB debug hardware from Nohau can be used with the IP2022.

Unobtrusive in-system programming is provided through the ISP interface. There is no need for a bond-out chip for software development. This eliminates concerns about differences in electrical characteristics between a bond-out chip and the actual chip used in the target application. Designers can test and revise code on the same part used in the actual application.

1.3.8 Applications

The IP2022 Internet Processor™ is optimized for network connectivity applications, and is ideally suited for use in the node and bridge/gateway portions of the Internet infrastructure.

Node device applications are those that are commonly associated with the “embedded Internet,” such as home appliances, medical devices, vending machines, and remote monitoring and control systems. These nodes are frequently interconnected by local-area networks (LANs). Bridge/gateway devices provide the functions that are required to connect the nodes, and their related LANs, to the Internet, such as protocol conversion, IP address routing, and firewall functions. The IP2022 enables true single-chip device and bridge/gateway connectivity implementations at a consumer price point. The library of ipModules, including the Internet protocol stack and communication inter-faces, allows design engineers to embed Internet connectivity in all of their products at low cost with very fast time-to-market.