Rev 2.2

Summary of Differences Between SX18/20/28 and SX48/52BD Production Release

	SX18/20/28AC	SX48/52BD
Compatibility Features	User selectable clock to instruction ratio of 1:1 or 1:4. User able to extend OPTION register to use all 8-bits (extra features) User able to extend stack size to 8-levels.	Clock to instruction ratio locked at 1:1. OPTION register fixed at 8-bit length. Stack size fixed at 8-levels.
Port Read	When read is performed from a bit position for a port, the operation is actually reading the voltage level on the pin itself.	Reading from a data register reads either the voltage level of the corresponding port pin or the data contained in the port data register depending on the status of PORTRD bit contained in the T2CNTB register.
Port Registers	Ports A/B/C LVL, PLP, and Direction registers are write only.	Ports A/B/C/D/E LVL, PLP, and Direction registers are read/write.
MODE Register	MODE register controls access to the port configuration registers. Bit 4 of the MODE register is not used and is initialized to 0.	MODE register not only controls access to the port configuration registers but also allows access to Timer T1 and Timer T2 registers. It also allows write operation to port configuration and timer registers. Bit 4 is used to perform read or write operation to configuration/status registers.
FUSE Word Register	Bits 11 used for selection of clock to instruction ratio. Bit 10 used for Synchronous input enable. Bit 7 used for Internal RC Oscillator enable. Bit 6 used to enable Internal Feedback Resistor Bits 5 and 6 used for Internal Oscillator divider selection. Bit 3 used for Code Protection enable. Bit 2 used enable Watchdog Timer. Bits 0,1 and 5 used for External Oscillator Gain selection.	All bits the same with the exception of: Bit 11 is unused.

FUSEX Word Register	Bits 8, 9, and 11 are used for internal RC oscillator trimming. Bit 10 is used for package selection. Bit 7 is used to enable 8-bit OPTION register and 8-level Stack. Bit 6 used for ADD/SUB with C enable. Bits 4 and 5 are used for Brown-Out-Reset. Bits 2 and 3 used for Brown-Out Reset Trimming. Bits 0 and 1 used for Program and Data Memory Size selection	All bits the same with the exception of: Bit 10 is used for Sleep Clock Disable. Bit 7 is unused. Bits 0 and 1 used for Delay Reset Timer period selection.
Delay Reset Timer (DRT) Timeout Period	Fixed delay for automatic wake-up from the power down mode.	A 2-bit field (DRT1: DRT0, bits 0 and 1)) at the FUSEX Word register can be used to specify the DRT timeout period that results in an automatic wake-up from the power down mode.
Sleep Clock Disable	Not available.	Bit 11 (SLEEPCLK) of the FUSEX word register is used to enable operation of the clock during the power down mode.
Program Memory	Organized as 2k, 12-bit wide words.	Organized as 4K, 12-bit wide words.
Program Counter	Upon reset, the program counter is initialized to 07FFh.	Upon reset, the program counter initialized to 0FFFh.
Data Memory	Consists of 136 bytes of RAM, organized as eight banks of 16 registers, plus an additional bank of 16 global registers, 8 of which are general-purpose RAM locations.	Consists of 262 bytes of RAM organized into 16 banks (banks 0 to F), each containing 16 registers, plus an additional bank of 16 “global” registers, 6 of which are general-purpose RAM locations.

Data Memory Addressing	The FSR register is used to specify the 3-bit bank number for direct addressing, or the full 8-bit address for indirect addressing. For direct addressing, the three high-order bits of FSR specify the bank number, and the instruction opcode ("fr" value) specifies the 5-bit address of the register within the selected bank. The five low-order bits of FSR are ignored in this addressing mode. For indirect addressing, the FSR register specifies the full 8-bit address of the register being accessed.	The data memory addressing can be divided into three categories: indirect, direct, and semi-direct. For direct addressing the 5-bit "fr" value within the instruction specifies the address to be accessed and the FSR register is ignored. For this addressing mode, only the global register bank is accessible. For indirect addressing, the FSR register specifies the register to be accessed. In this mode, the global register bank and Bank 1 through Bank F are accessible. Bank 0 is not accessible. For semi-direct addressing, the bank number is selected by the four high-order bits of FSR, and the register within that bank is selected the four low-order bits of "fr". Bank 0 through Bank F is accessible, but the global register bank is not accessible.
BANK Instruction	BANK instruction modifies bits 5, 6 and 7 of the FSR.	BANK instruction modifies bits 4, 5 and 6 of the FSR. FSR bit 7 is user selectable.
RTCC Rollover Interrupt Pending Bit	No RTCC rollover interrupt pending bit.	Offers RTCC rollover interrupt pending bit (RTCCOV bit in T1CNTB register).
16-bit Multi-Function Timers	None.	Contains Two.
Bidirectional I/O Ports	Ports A, B, C.	Ports A, B, C, D, E.
Interrupt Sources	RTCC, External (8 pins).	RTCC, External (8 pins), Timer T1, Timer T2.
Interrupt Context Shadow	FSR, STATUS, W and PC shadowed.	FSR, STATUS, W, MODE and PC shadowed.
Packages	18 SDIP/SOIC, 20 SSOP, 28 SDIP/SOIC, 28 SSOP	48 TQFP, 52 PQFP