NEC

Fact Sheet

NA70008H
Embedded Megamacro
Z80® Compatible 8-Bit CPU

January 1993

NA70008H Megamacro

The NA70008H embedded megamacro is an industry-standard 8-bit CPU building block for use in CB-C7 cell-based CMOS ASIC designs. It is fully compatible with NEC's μPD70008 standard part and functionally compatible with the industry-standard Z80® CPU. It is ideal for many embedded applications, such as industrial control, handheld terminals, and cellular phones, where a cost-effective microprocessor is needed.

The NA70008H is an 8-bit central processing unit that offers high system throughput and efficient memory utilization. As shown in figure 2, there are three groups of registers within the CPU. The first group consists of duplicate sets of 8-bit registers; a principal set and an alternate set. Both sets consist of the Accumulator Register, the Flag Register, and six general-purpose registers. Transfer of data between these duplicate sets of registers is accomplished by means of "Exchange" instructions. The result is faster response to interrupts and efficient implementation of such versatile programming techniques as background-foreground data processing.

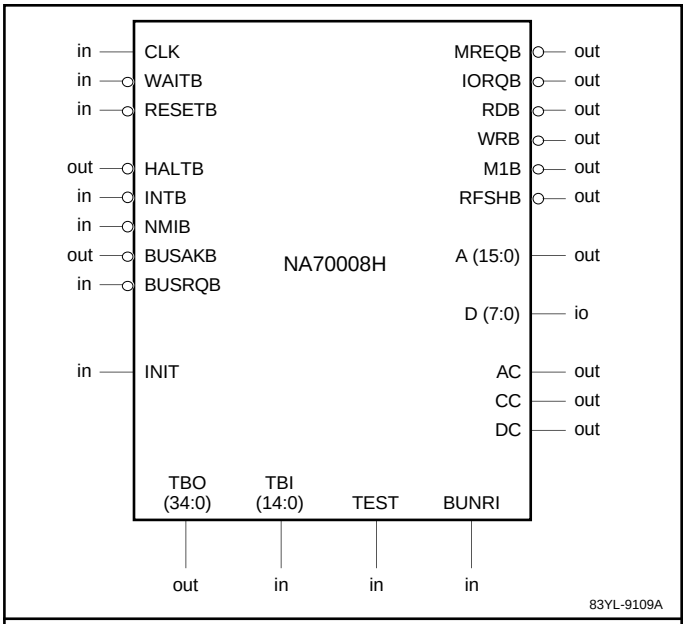
The instruction set also includes such operations as a block move for fast data transfers within memory or between memory. It also allows operations on any bit in any location in memory.

Designing with embedded megamacros facilitates a cell-based design. They are easy to place, route to, and to simulate, especially if the designer is already familiar with the megamacro's functions. By using these pre-characterized and pre-laid out cells, a higher level starting point is possible, which can result in a considerable savings in design time. A unique test bus architecture allows complete but separate testing of the internal circuit of the NA70008H, in isolation from the user logic, during final device test.

Features

- □ Full complement of Z80 instructions (158 total)
- □ 64 kilobyte direct map memory address
- □ Non-maskable and maskable interrupts
- □ Dynamic memory refresh counter
- □ 17 interrupt registers
- □ High performance 0.8 μm CZ-IV CMOS process

Figure 1 NA70008H Symbol and I/O Identification



I/O Signals	Description	Capacitance - pF (Fan-in/out)
CLK	Clock input	0.11 (0.68)
WAITB	Wait input	0.11 (0.68)
RESETB	Reset input	0.11 (0.68)
HALTB	Halt state	6.50
INTB	Interrupt request	0.10 (0.67)
NMIB	Non-maskable interrupt	0.11 (0.68)
BUSAKB	Bus acknowledge	6.50
BUSRQB	Bus request	0.11 (0.68)
INIT	Initialization input	TBD
MREQB	Memory request	9.35
IORQB	Input/Output request	9.35
RDB	Read strobe output	9.35
WRB	Write strobe output	9.35
M1B	Machine cycle one	6.50
RFSHB	Refresh	6.50
A(15:0)	Address bus	9.36
D(7:0)	Data bus	0.21 (0.78)/9.25
TBI(14:0)	Test bus inputs	0.11 (0.68)
TBO(34:0)	Test bus outputs	9.35
TEST	Mode switch pin for test bus	0.11 (0.68)
BUNRI	Mode switch pin for test bus	0.21 (0.78)
AC	Control for address bus 3-state enable	6.50
CC	Control bus 3-state enable	6.50
DC	Data bus control	6.50

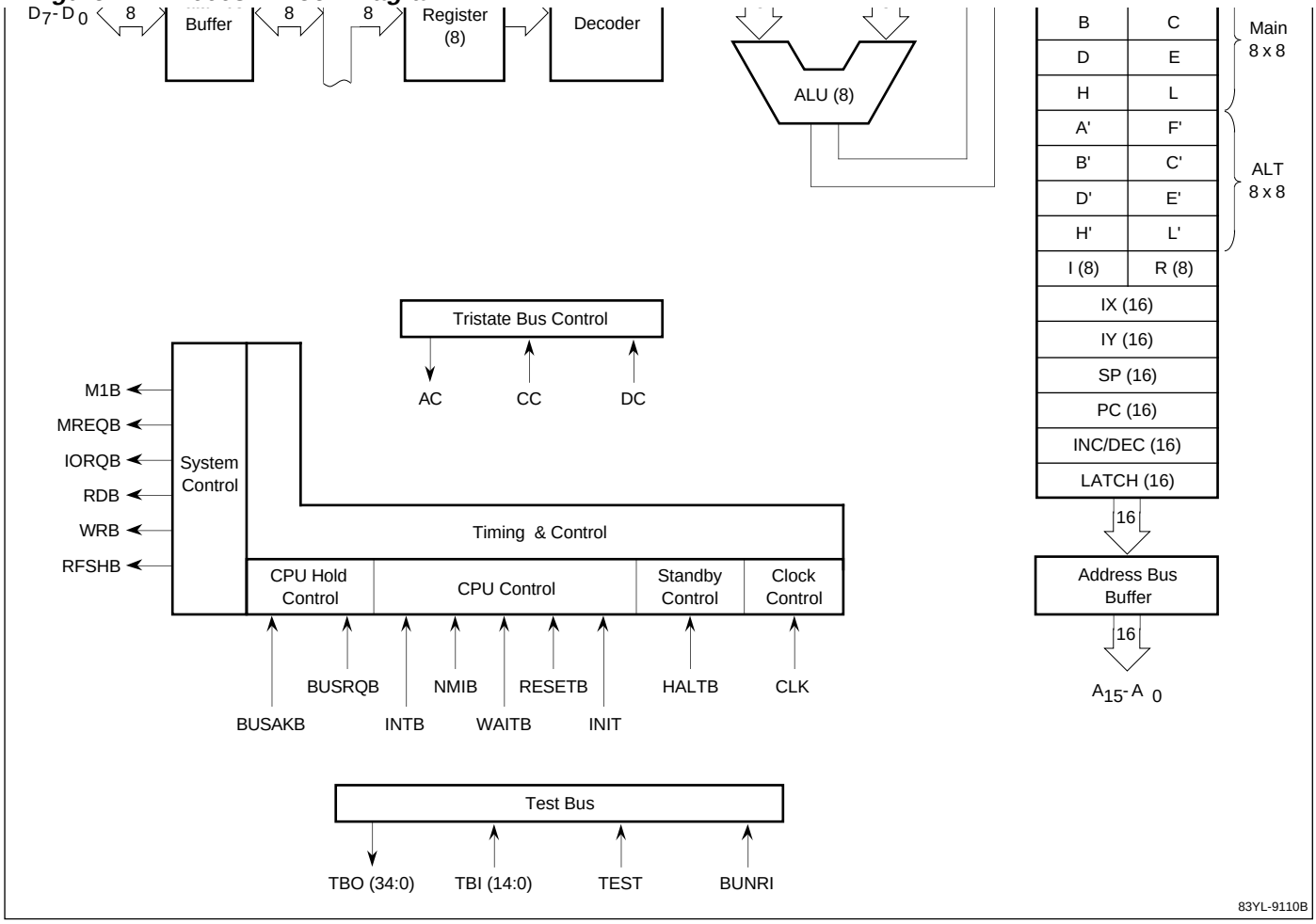
Note: Fan-in conditions are given in parenthesis
Stand-alone values are output capacitances in pF, and also represent the fan-out

Specifications

Parameter		Conditions
Grid area	40,250	includes VDD and GND ring
Operating frequency	16 MHz (max) @5V; 8MHz (max) @ 3V	
Operating current	Under Evaluation	
Power dissipation	Under Evaluation	
Number of separate simulation test patterns	TBD	

Z80 is registered trademark of Zilog, Inc.

Figure 2 NA70008H Block Diagram



NEC Electronics Inc.

CORPORATE HEADQUARTERS

475 Ellis Street
P.O. Box 7241
Mountain View, CA 94039
TEL 415-960-6000

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or FAX your request to: **1-800-729-9288**
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