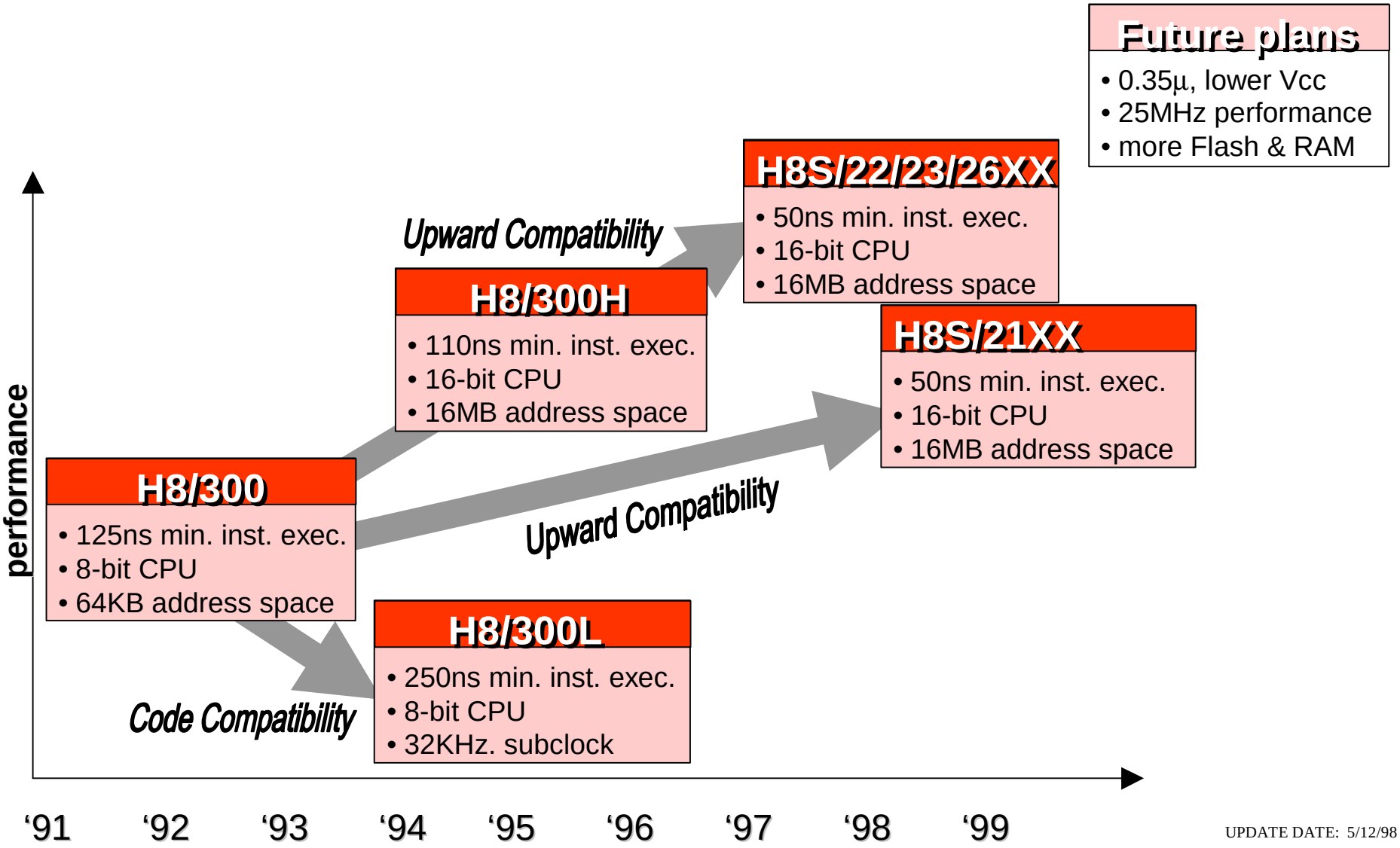
8 & 16-bit CISC Architectures
Technical Product Overview

H8 Family Roadmap
Over $1B in Sales



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H8 Performance Factors

Integration, Low Power, and Performance

Memory and Peripheral ***Integration***

- Large blocks of on-chip memory: Flash, OTP, ROM - 128KB
- Abundant on-chip peripherals: LCD, I^2C, SCI, Timers, A/D, DRAM Ctrl

Low Power Design Techniques and Features

- Up to 7 different low power modes provided
- Peripheral “modular” power down
- Low voltage operation - down to 2.2V
- Static design (H8S) and 32KHz clock option

Leading ***Performance*** in the 8/16-bit MCU Class

- Min. 50nsec instruction execution time @ 20 MHz operation

Preserves Your S/W Investment

- Excellent C language support with a register-based, load/store architecture
- A wide range of price/performance solutions offering an easy migration path from low-end 8-bit to high-end 16-bit solutions

Hitachi 8 & 16 Bit Micro Overview

Family	Architecture	MIPS	Key Features
H8/300L	**8 bit**	**1.0 MIP**	• Integrated LCD/Vacuum Fluorescent Drivers • 32 KHz sub-clock with 7 low-power modes • A/D, watchdog timer, PWM, SCI • Up to 8 MHz operation • 2.2-5.5V
H8/300	**8 bit**	**2.0 MIPS**	• 64Kbytes address space • host interface/keyboard control functions • I^2C bus interface • A/D, watchdog timer, PWM, SCI • Up to 16 MHz operation • 2.7-5.5V
H8/300H	**16 bit**	**4.0 MIPS**	• 16MB of linear address space • DMAC: Direct Memory Access Controller • A/D, D/A, WDT, ITU, TPC, SCI, Smart Card • direct interface to DRAM (RAS, CAS, CS) • up to 18 MHz operation • 2.7-5.5V
H8S/2000	**16 bit**	**10.0 MIPS**	• static core with 32 KHz sub-clock • Burst ROM, fast page DRAM support • DMAC, A/D, D/A, TPU, PPG, SCI, WDT • multiply and accumulate unit: 16x16+42 bit • up to 20 MHz operation • 2.7-5.5V

WDT = watchdog timer
ITU = integrated timing unit
TPU = timer pulse unit
TPC = timing pattern controller
SCI = serial communication interface
PPG = programmable pattern generator

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Topics

H8/H8S CPU Architecture

- Register Structure
- Addressing Modes
- Instruction Set
- Processing States
- Access Timing
- Operation Modes
- Power Down Modes

On-chip Memory

General-purpose I/Os

8-bit CISC Peripherals

- H8/300L and H8/300
- Interrupt Processing

16-bit CISC Peripherals

- H8/300H and H8S
- Interrupt Processing

H8/H8S CPU

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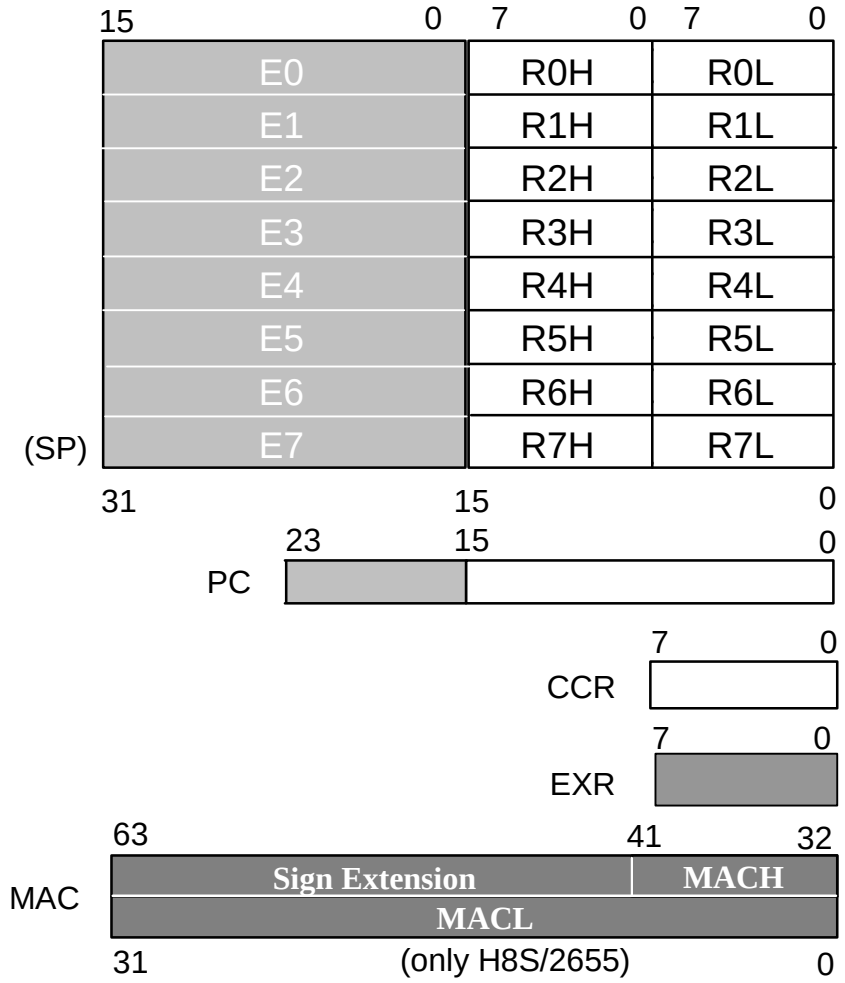
CPU Structure

General purpose registers

- 8, 16, or 32-bit length
- No restrictions on usage
- Used as accumulator, index register, address pointer, or data storage

Load/store architecture

- Register-to-register operations
- Supports high level (C) efficient programming



PC = Program Counter
CCR = Condition Code Register
EXR = Extended Control Register
MAC = Multiply-Accumulate Register
SP = Stack Pointer

H8/300L & H8/300 — Added to H8/300H & H8S/2000 — H8S/2000 only

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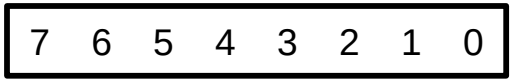
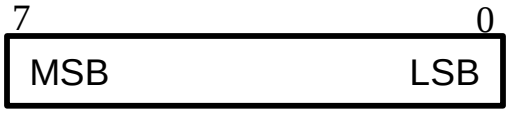
Data Formats in Memory

Data Type	Address	Data Format
1-bit Data	Address “A”	
Byte Data	Address “B”	
Word Data	Address “C”	
	Address “C+1”	
Longword Data	Address “D”	
	Address “D+1”	
	Address “D+2”	
	Address “D+3”	

H8/300H and H8S ONLY

Addressing Modes

- Register direct
- Register indirect
- Register indirect with displacement
- Register indirect with post-increment
- Register indirect with pre-decrement
- Absolute address
- Immediate
- Program counter relative
- Memory indirect

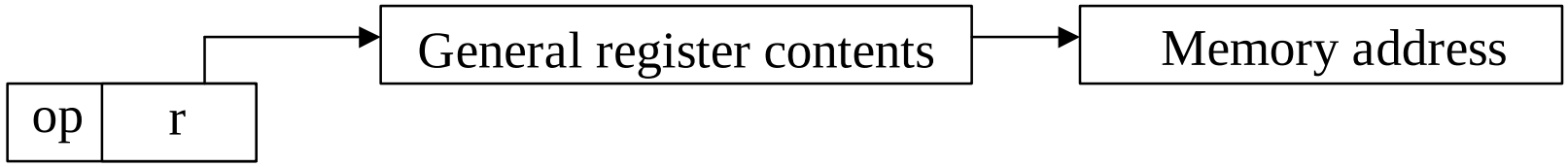
Addressing Modes (cont'd.)

Register Direct

- Operand is general register contents.
- e.g. MOV.W R0,R1

Register Indirect

- Effective address of operand given by contents of general register in the instruction code.
- e.g. MOV.B R0L,@R0H

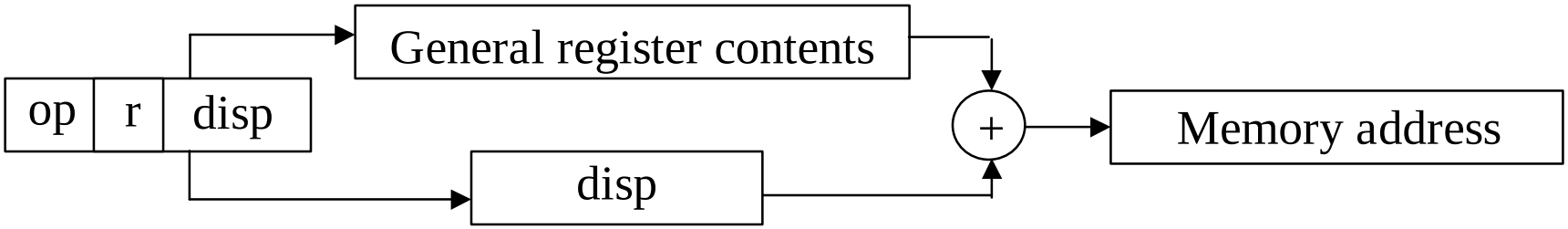


Addressing Modes (cont'd.)

Register Indirect with Displacement

- Effective operand address calculated by adding a displacement to a general register contents, both contained in the instruction code
- e.g. MOV.W @(h'7FFF,ER0), R1

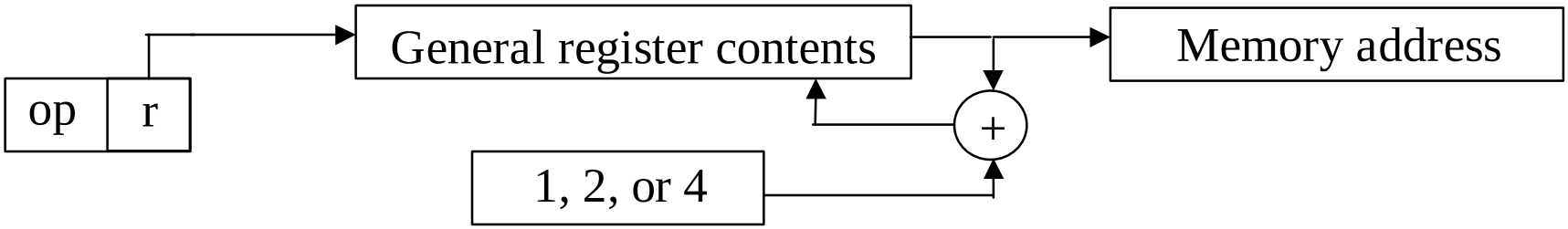
- Displacement size16-bit for H8/300L-300, 16/24-bit for H8/300H, 16/32-bit for H8S/2000



Addressing Modes (cont'd.)

Register Indirect with Post-Increment

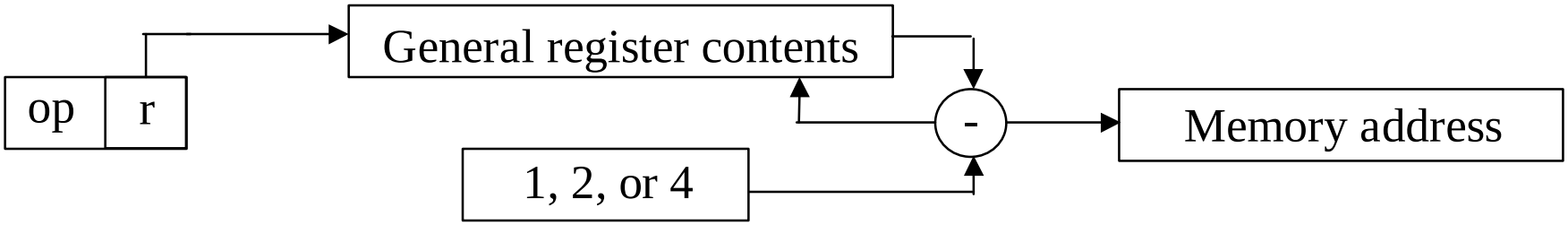
- Effective address of operand is in the contents of a general register specified in the instruction code. After the operand is accessed, the specified general register is incremented by 1,2,or 4
- e.g. MOV.L @ER0+, ER1



Addressing Modes (cont'd.)

Register Indirect with Pre-Decrement

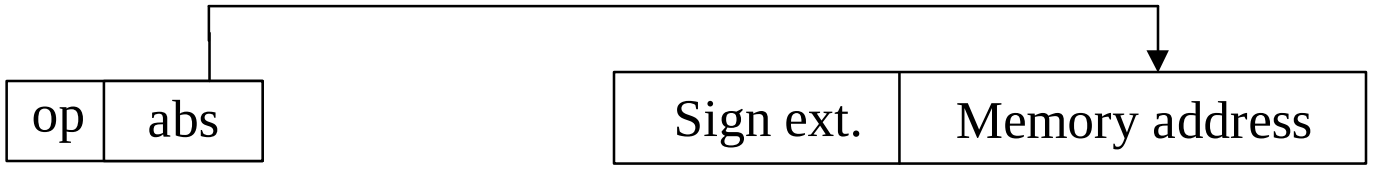
- Effective address of operand is calculated by decrementing 1,2,or 4 from the contents of a general register specified in the instruction code
- e.g. MOV.W R0, @-ER1



Addressing Modes (cont'd.)

Absolute Address

- Effective address of operand is in the instruction code
- e.g. MOV.W @h'7D00, R0



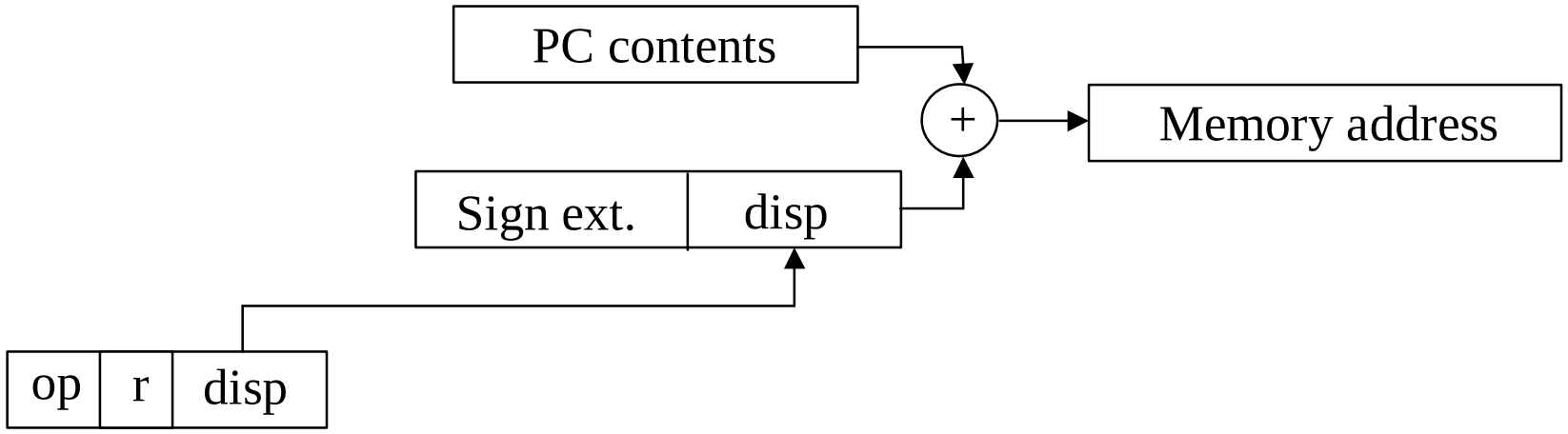
Immediate

- Operand is immediate data
- e.g. MOV.W #h'FFE0, R0

Addressing Modes (cont'd.)

Program-Counter Relative

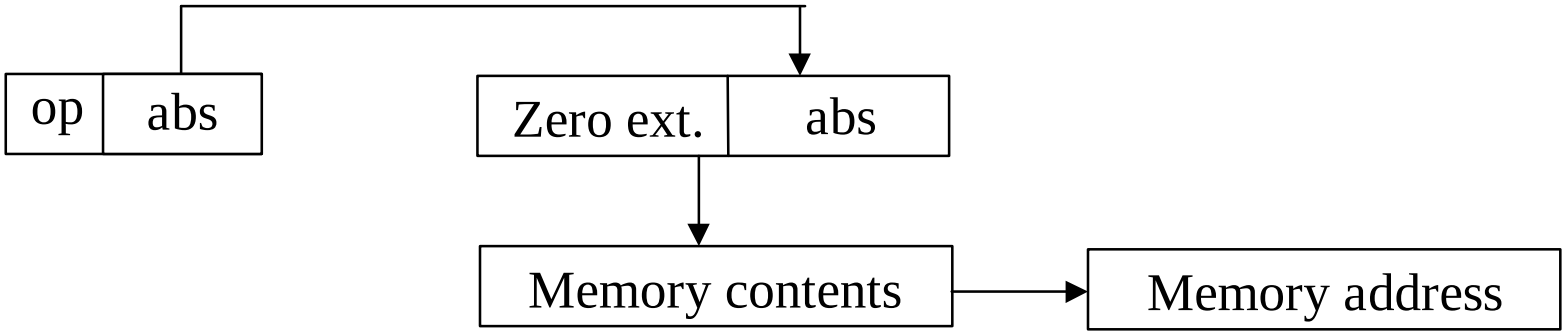
- Effective address of operand is in the instruction code to which the contents of the PC are added. e.g. BSR h'7F



Addressing Modes (cont'd.)

Memory Indirect

- Effective address of operand is contained in a memory location pointed from the instruction code. e.g. JMP @@h'E5

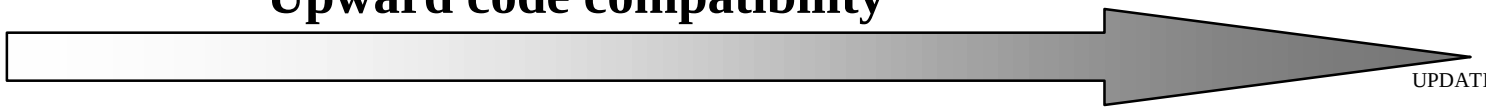


Instruction set

Types of Operations	H8/300L	added to H8/300	added to H8/300H	added to H8S/2000
Data transfer	MOV, POP, PUSH	MOVFPE, MOVTPE		LDM, STM
Arithmetic Operations	ADD, SUB, ADDX, SUBX, INC, DEC, ADDS, SUBS, DAA, DAS, MULXU, DIVXU, CMP, NEG		MULXS, DIVXS, EXTS, EXTU	TAS **MAC, LDMAC, STMAC, CLRMAC***
Logical Operations	AND, OR, XOR, NOT		Word & long word support	Word & long word support
Shift	SHAL, SHAR, SHLL, SHLR, ROTL, ROTR, ROTXL, ROTXR			
Bit manipulation	BSET, BCLR, BNOT, BTST, BAND, BIAND, BOR, BIOR, BXOR, BIXOR, BLD, BILD, BST, BIST			
Branch	Bcc, JMP, BSR, JSR, RTS (Bcc = conditional branch on cond. "cc")			
System control	RTE, SLEEP, LDC, STC, ANDC, ORC, XORC, NOP		TRAPA (software interrupt)	
Block data transfer	EEPMOV			

*** Multiply And Accumulate (MAC) instructions on H8S/26XX family w/ hardware MAC unit only**

Upward code compatibility



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Min. Instruction Execution Time

Options	H8/300L	H8/300	H8/300H	H8S
Internal memory	2 states	2 states	2 states	1 state
External memory	N/A	3 states	2 states	2 states
Max. frequency	8MHz	16MHz	18MHz	20MHz
Min. exec. time	250ns	125ns	110ns	50ns
% of instructions	50%			

CPU Processing States

Program Execution

- Program instructions executed in sequence by CPU

Exception Handling

- Transient state where normal processing flow is changed in response to an exception

Bus-Release

- Bus mastership relinquished by CPU

Power Down

- CPU and/or peripheral operation stopped

Data Access Timings

H8/300L and H8/300

- Fixed as in the table below
- Certain H8/300 devices allow wait-state insertion

H8/300H and H8S

- adjustable in the Bus Controller

Options	H8/300L		H8/300		H8/300H		H8S/2000	
	Bus width	Min # cycles	Bus width	Min # cycles	Bus width	Min # cycles	Bus width	Min # cycles
On-chip memory	16-bit	2	16-bit	2	16-bit	2	16-bit	1
On-chip peripherals	8-bit	2 or 3	8-bit	3	8/16-bit	3	8/16-bit	2
External memory	N/A	N/A	8-bit	3[1]	16-bit	2	16-bit	2

1. **Word transfers are executed in 6 cycles.**

Operating Modes

Single-chip Modes

- All address space mapped within the MCU

Expanded Modes

- Address space mapped externally and within the MCU

Mode features	H8/300L		H8/300		H8/300H		H8S	
	Single-chip	Expanded	Single-chip	Expanded	Single-chip	Expanded	Single-chip	Expanded
Max. addressability	64Kbytes*	N/A	64Kbytes*	64Kbytes	1Mbyte*	16Mbytes	16Mbytes*	16Mbytes
Max. # of modes	1	N/A	1	2	1	6	2	5

* actual on-chip memory is smaller

Power Down Modes

Sleep Mode

- Clock runs, CPU stops, but CPU/Peripheral registers held

Software Standby

- Clock stops, only CPU registers and RAM contents held

Hardware Standby

- Clock stops, only RAM contents held
- Not available on H8/300L

Medium Speed

- Bus master operates on slower clock, peripherals operate normally
- On all families except the H8/300

Subsleep/Watch

- CPU halts, only timer channel(s) operate on the 32KHz subclock
- Only on H8/300L and H8S

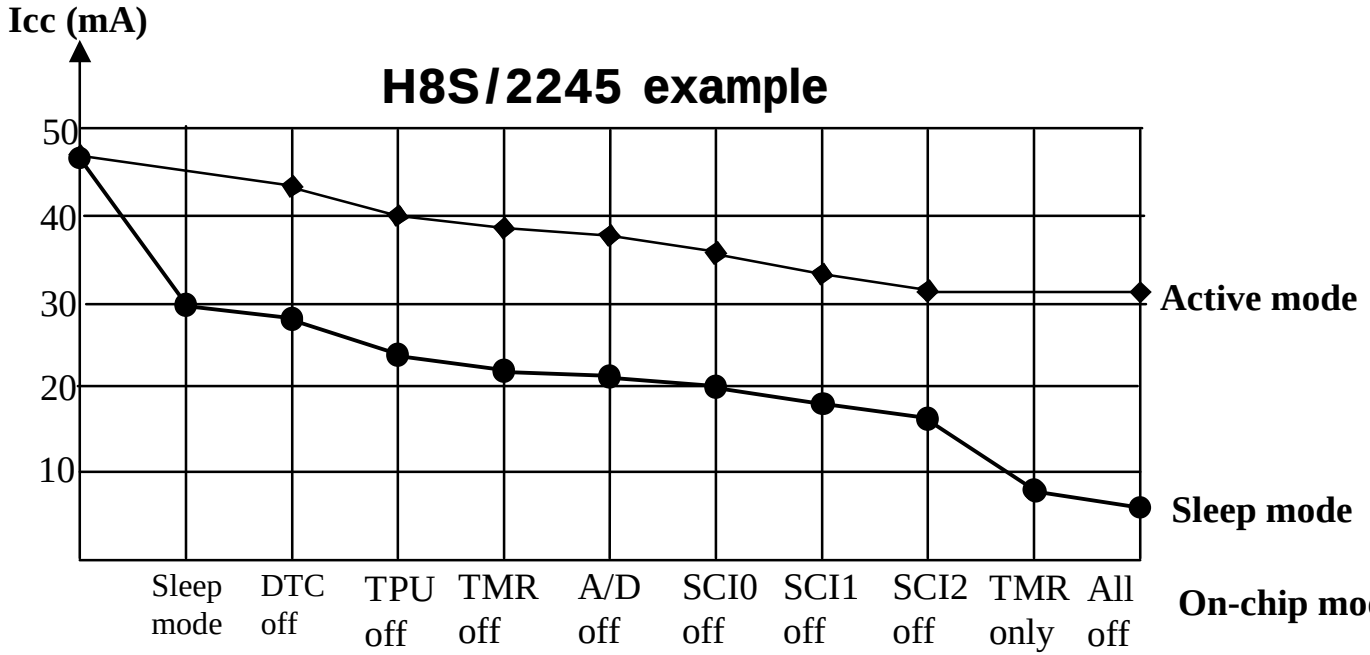
Power Down Modes (cont'd.)

Subactive

- 32KHz subclock operation for CPU and a timer channel
- Only on H8/300L and H8S

Module Standby

- Halting one or several peripherals
- Not available on H8/300L-300



Power Down Modes (cont'd.)

Typical Power Consumption at 3V

MODES	H8/300L		H8/300		H8/300H		H8S	
	typ	max	typ	max	typ	max	typ	max
Sleep mode	6mW	9mW	27mW	48mW	36mW	72mW	27mW	92mW
Software standby mode	30nW	15µW	30nW	15µW	30nW	15µW	30nW	15µW
Hardware standby mode	-	-	30nW	15µW	30nW	15µW	30nW	15µW
Watch mode (32KHz subclock oscillator)	N/A	18µW	-	-	-	-	N/A	N/A
Subsleep mode	15µW	30µW	-	-	-	-	N/A	N/A
Medium speed active mode	3mW	N/A	-	-	-	-	N/A	N/A
Subactive mode (32KHz subclock oscillator)	30µW	60µW	-	-	-	-	N/A	N/A
Module standby/stop mode	-	-	-	-	21mW	42mW	N/A	N/A

1. The measurements above are for the following specific devices: H8/3644 (300L), H8/3437 (300), H8/3048 (300H), and H8S/2245 (H8S).
2. Power dissipation numbers are measured at the MAXIMUM operating frequency at 3V.
3. H8/300H and H8S also support 'CLOCK GEARING-DOWN" - software programmable clock division.
4. N/A: data not available
5. - : not applicable

On-chip Memory

High density ROM, Flash, RAM

- Over 100 memory configuration options available

Maximizes performance

- On-chip memory access is FASTEST

Minimizes system power consumption and board space

Maximum Available Densities

H8 Family	Flash	OTP	Mask ROM	Romless	RAM
H8/300L	32KB	60KB	60KB	N/A	2KB
H8/300	60KB	60KB	60KB	✓	4KB
H8/300H	128KB	256KB	256KB	✓	4KB
H8S	128KB	128KB	128KB	✓	8KB

Flash vs. OTPs - Advantages

Single cycle access to internal memory

Lower system power

- less bus state controller utilization
- single chip powered vs. two

Lower development cost

- Flash can be programmed/erased instead of discarding multiple OTPs

Lower manufacturing cost

- scrapping of OTPs due to code changes can be eliminated

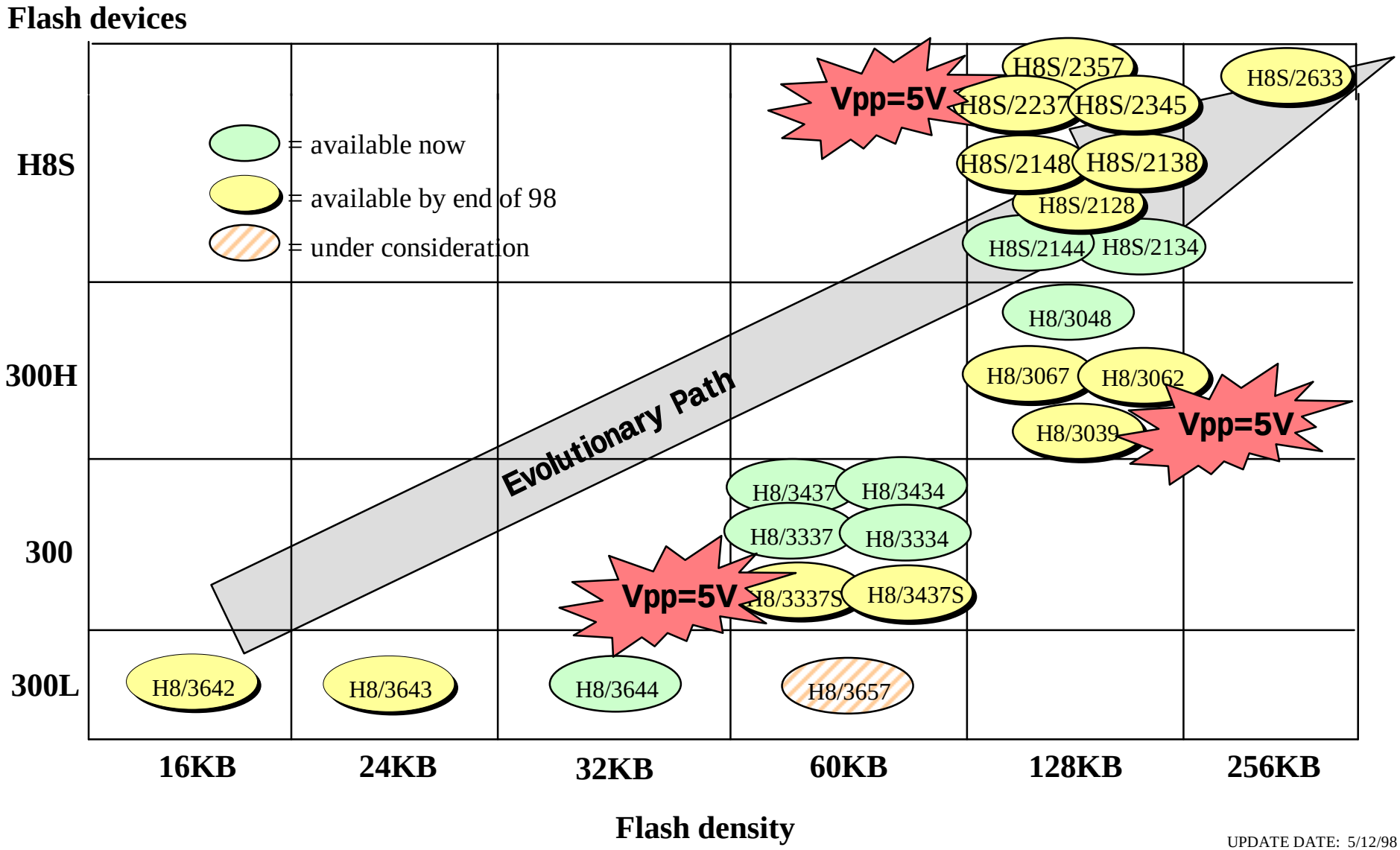
Initial flexibility during manufacturing

- a single end product can be “personalized” at final assembly or test for different customers or end-markets

After-shipment software upgrades

- end product can be modified repeatedly in the field

H8/H8S Flash Roadmap



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Flash General Features

Programming voltage

- 0.8µ devices require 12V programming voltage
- 0.5µ devices require 5V programming voltage - NOW AVAILABLE

Efficient block programming and erasing

- Memory area partitioned in block sizes from 512 bytes up to 32Kbytes

Fast programming and erasing

- 50µs per byte programming and 1sec. total erasure time

100 reprogramming cycles guaranteed

A variety of programming channels

- Via SCI, I^2C, IrDA, or parallel interface

Flash Operation-Control Modes

The steps involved during the pre-programming and programming processes

Program mode

- Writes data to the flash memory

Program verify mode

- Data in flash is verified

Erase mode

- Erase block(s) of flash

Erase verify mode

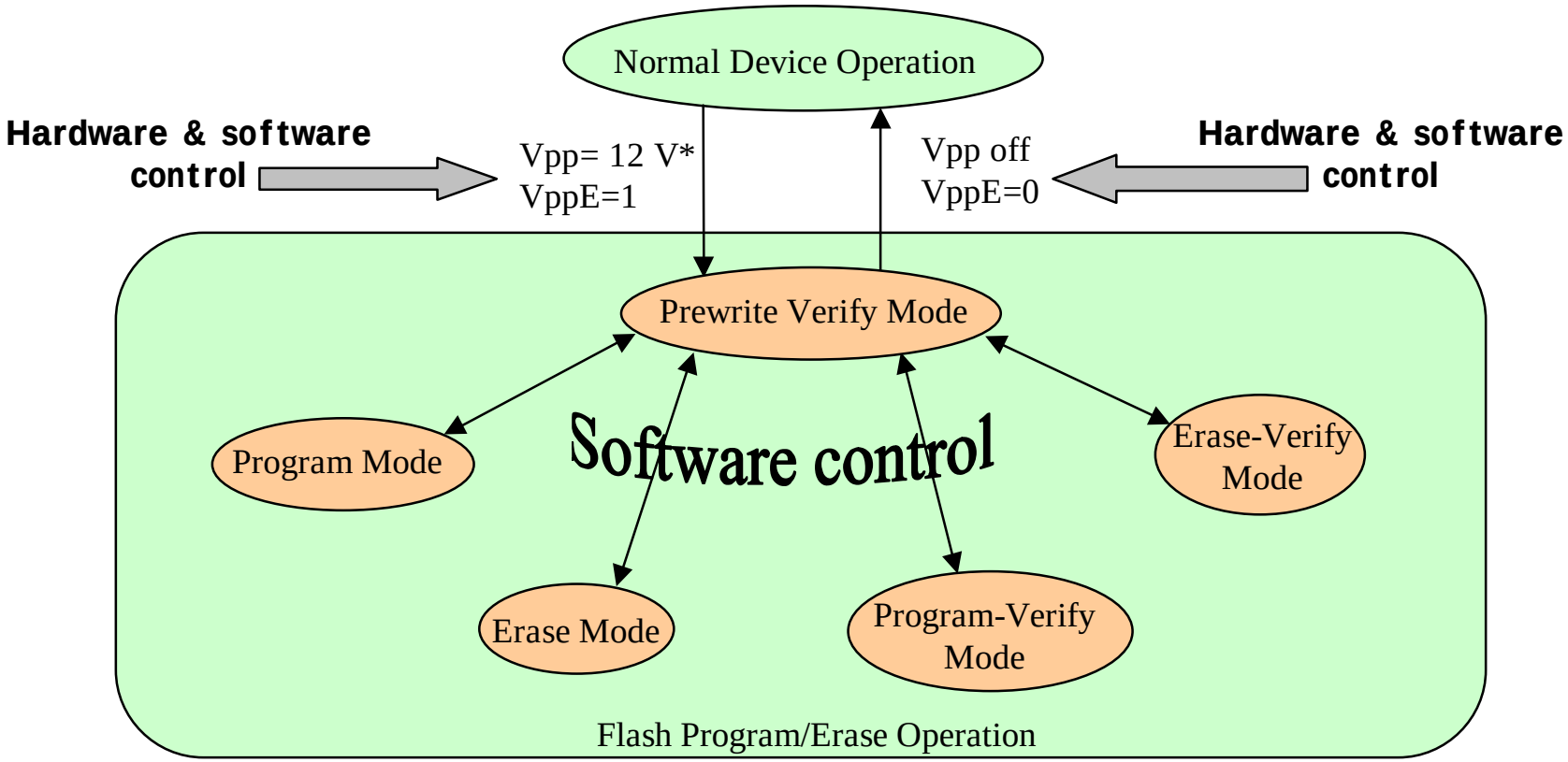
- Check flash is erased

Prewrite verify mode

- Verifies all flash cells are “0”

Flash Programming Process

Flash Memory Program/Erase Operating Mode State Transition Diagram



* = New devices have single-voltage (5V) flash - no separate Vpp programming voltage necessary

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Flash Programming Modes

Methods to load the application code into the flash memory

PROM Mode

- Uses programming adapter in PROM programmer

BOOTSTRAP Mode

- Serially programs from host using built-in bootstrap loader via SCI

User Program Mode

- Device programs itself according to user application

PROM Mode

Will program on an EPROM programmer using programming socket adapter*

Electronic Erase

Fastest way for production programming

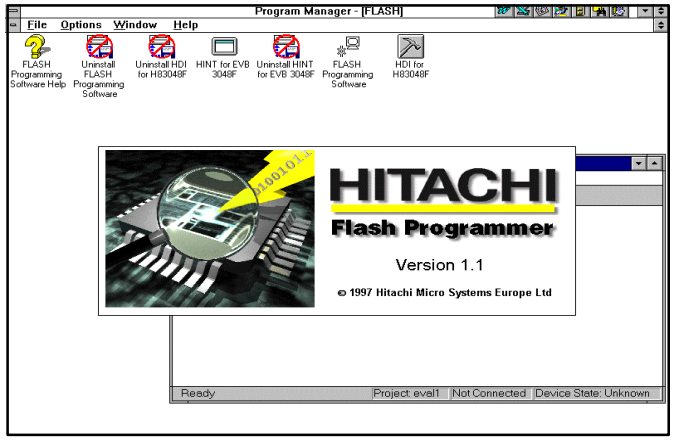
- 49 sec for H8/3334Y on Data I/O Unisite
- Sub 10 seconds possible on some programmers

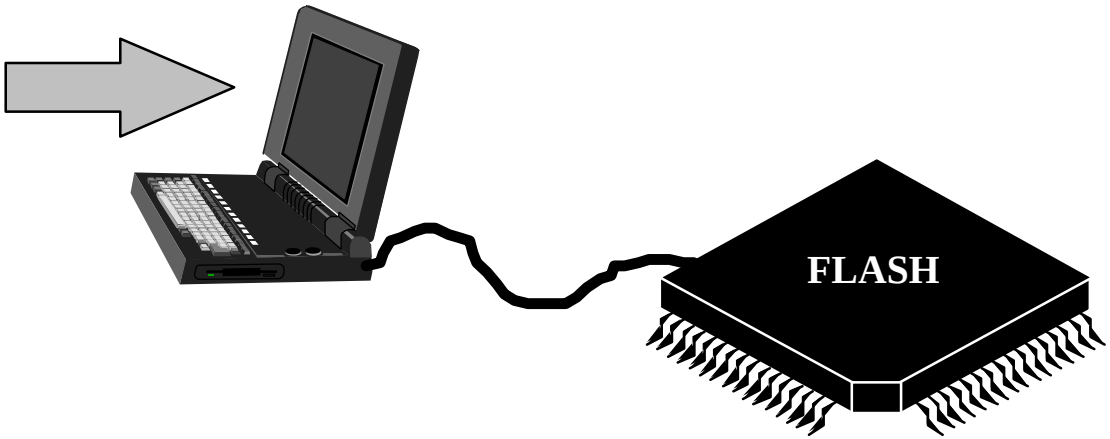
Security bit function

Require specific device algorithm - most programmers support Flash devices

* available from Hitachi, Data I/O, or BP Microsystems

Bootstrap Mode



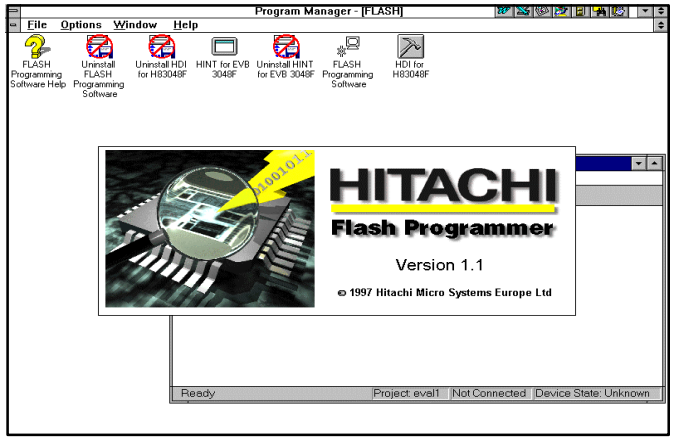


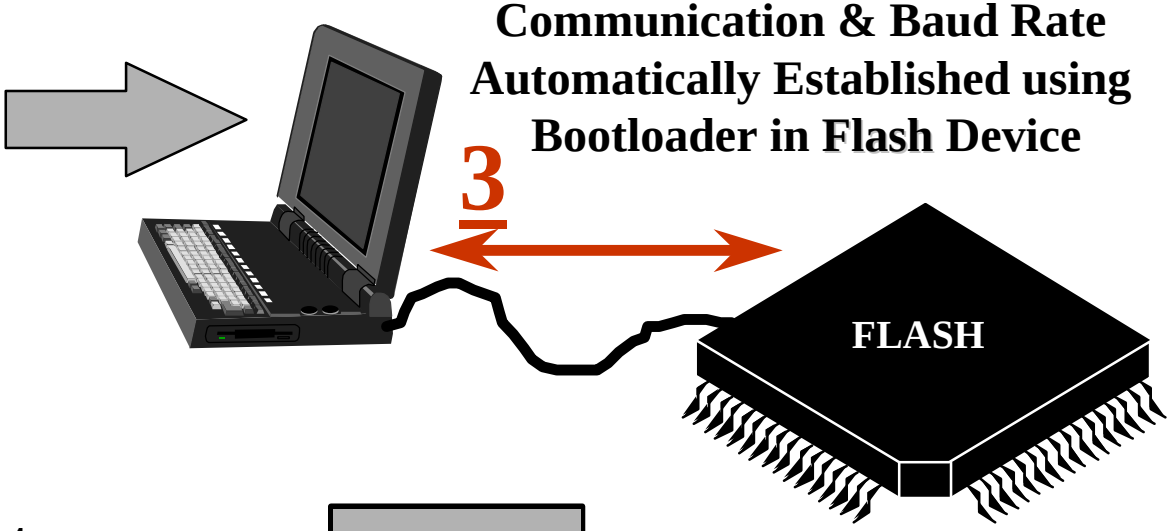
Features

- Allows a host processor to download any application via SCI to RAM which will then execute
- Great for in-circuit programming
- Great for system test and similar applications
- Flash is erased before download (and verified to be erased)
- Flash may be reprogrammed with security bit set

No Pre-Programmed Boot Strap Required - Already Coded

Bootstrap Mode (cont'd.)





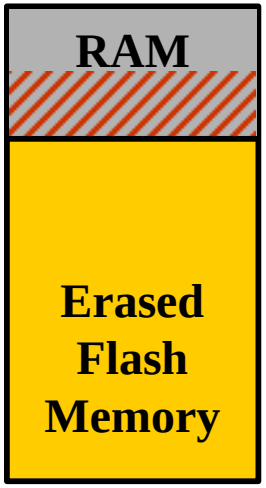
Communication & Baud Rate Automatically Established using Bootloader in Flash Device

3

1 **Apply Boot Mode Conditions to External Pins and Reset**

Erase Complete Flash Memory

2



Memory Map

4

Flash Programming Kernel Loaded via serial port

5

Kernel is Executed From RAM and loads the flash memory with the application code

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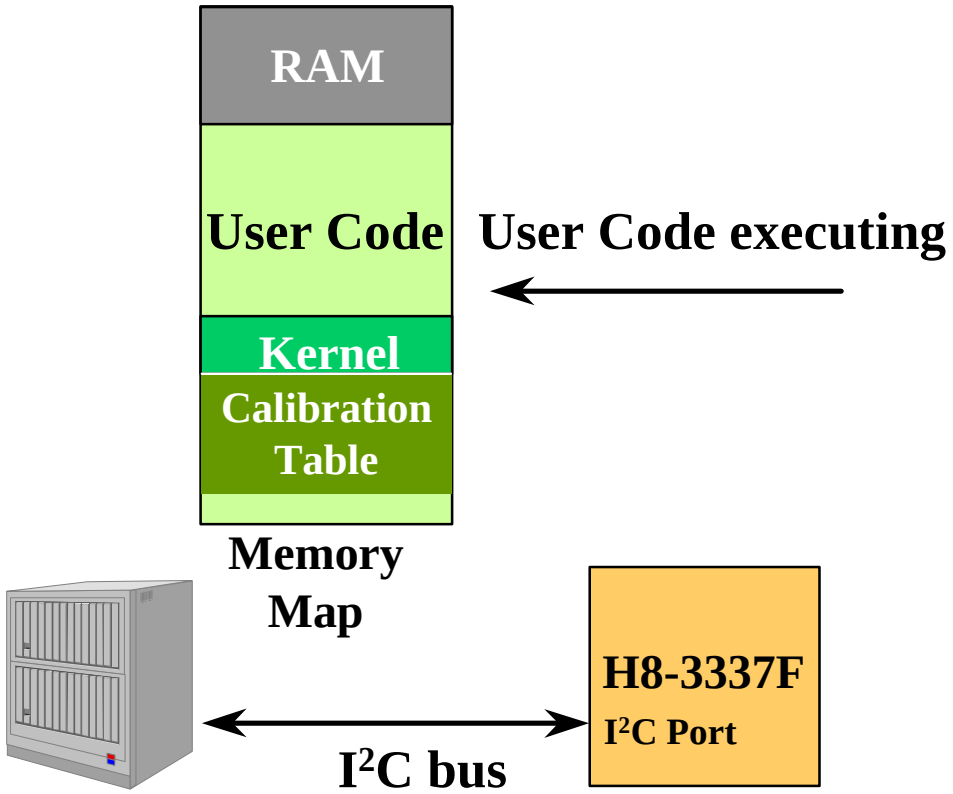
User Program mode

- Allows just flash blocks to be programmed rather than complete Flash memory (Boot Mode)
- Allows the programming of the flash under the user kernel control
- Allows the download of new program data by a method defined by user, e.g. parallel port, I^2C, or IrDA (not just the SCI)
- The user has complete control of the programming process
- Security is up to the users application

User Program Mode Example

- **H8-3337 FLASH Device**
- **USER Software kernel linked with users' code**
- **Require to reprogram 512 byte block with new calibration table**
- **New calibration table loaded via I²C port from host**

- Microcontroller running normally
- Signal that new calibration table is required from Host via I²C bus
- Flash programming kernel copied from onboard flash to internal RAM by users' code
- Users' code jumps to kernel & begins execution, 12v controlled via I/O pin under kernel control (first saving SP)
- Flash block erased & verified
- Data is read from I²C port and programmed byte by byte & verified
- Jump back to normal operation (After restoring SP !)



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General-Purpose I/Os

Memory-mapped and accessed via dedicated data registers

H8/300L and H8/300

- Up to 74 I/O lines
- Up to 16 capable of driving LEDs

H8/300H and H8S

- Up to 87 I/O lines
- Up to 40 capable of driving LEDs

Multiplexed with various module functions

TTL load and Darlington pair driving capability

8-bit CISC Peripherals

- H8/300L and H8/300
- Interrupt Processing

8-bit CISC Peripheral Modules

Modules	H8/300L	H8/300
16-bit Timer(s)	✓	✓
8-bit Timer(s)	✓	✓
PWM(s)	✓	✓
Watchdog Timer	✓	✓
Serial Communication Interface	✓	✓
I^2C Interface		✓
A/D Converter	✓	✓
D/A Converter		✓
LCD Controller	✓	
Host Interface Controller		✓

16-bit Free Running Timer (FRT)

One channel (H8/3318 has 2 channels)

Two independent comparators per channel

- Up to 2 simultaneous waveforms per channel

Four input-capture lines (H8/3318 has 5)

- Current count can be captured on rising/falling edge of input signal
- Two channels can be used as buffers for the other 2 channels

Counter clear option - upon compare-match

Selection of 4 clock options

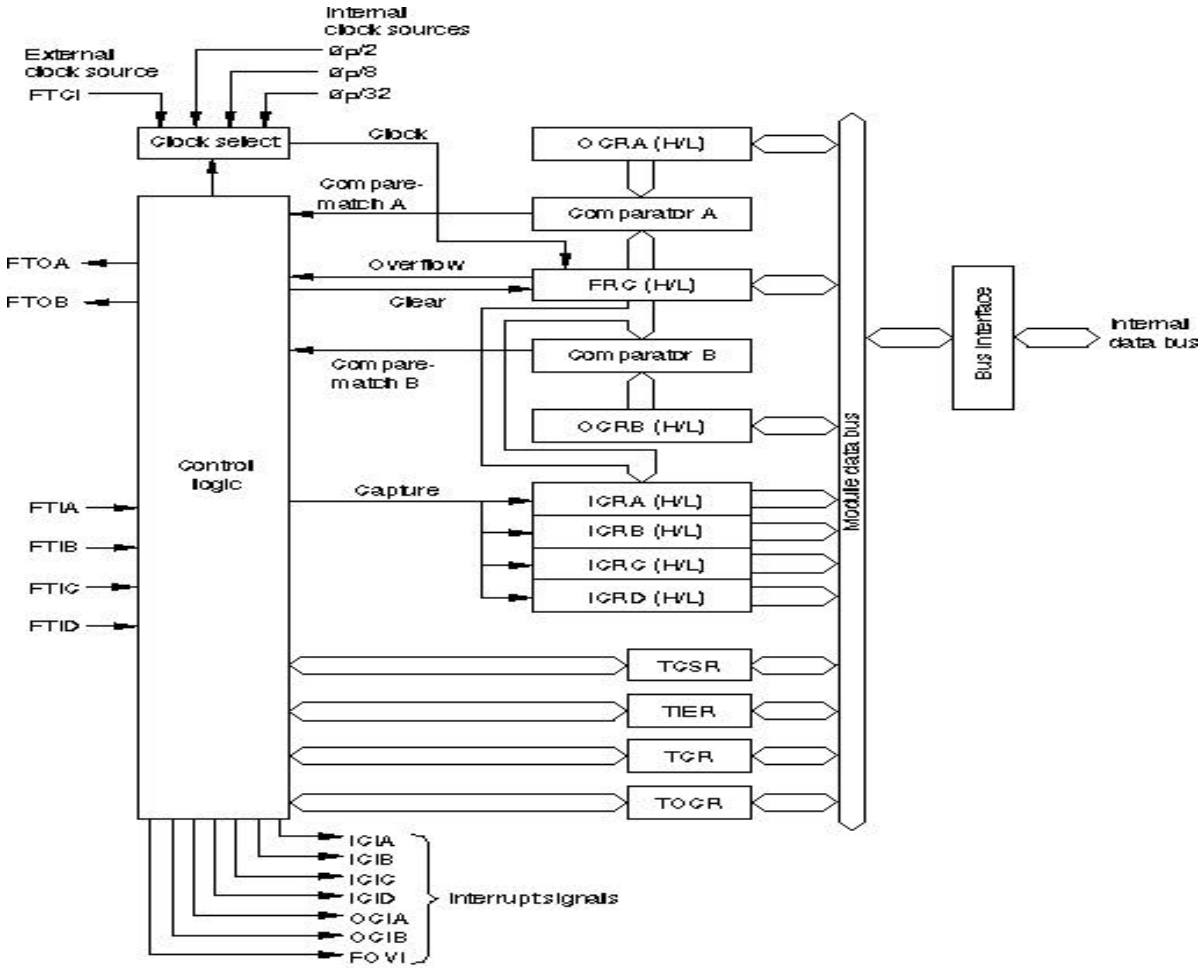
- 3 internal and 1 external

Interrupt-generating capability

- Upon compare-match, input-capture, and/or overflow

16-bit FRT Block Diagram

H8/3437 example



Legend

FRC:	Free-running counter (16 bits)	TIER:	Timer interrupt enable register (8 bits)
OCRA, B:	Output compare register A, B (16 bits)	TCR:	Timer control register (8 bits)
ICRA, B, C, D:	Input capture register A, B, C, D (16 bits)	TOCR:	Timer output compare control register (8 bits)
TCSR:	Timer control/status register (8 bits)		

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8-bit Timers

Type One (on H8/300L only)

- One channel
- Operates as an interval timer - interrupt generated upon overflow
- Provides real-time clock base operation
  - uses 32KHz subclock as count base for 4 distinct overflow periods
  - interrupt generated upon overflow
- Can output 8 clock signals - 4 derived from the 32KHz subclock, and 4 derived from the system clock

Type Two (on H8/300L only)

- One channel
- Operates as an interval timer - interrupt generated upon overflow
- Provides software-controlled auto-reload function - new timer value loaded from load value register
- Timer clock sources - 7 internal and 1 external

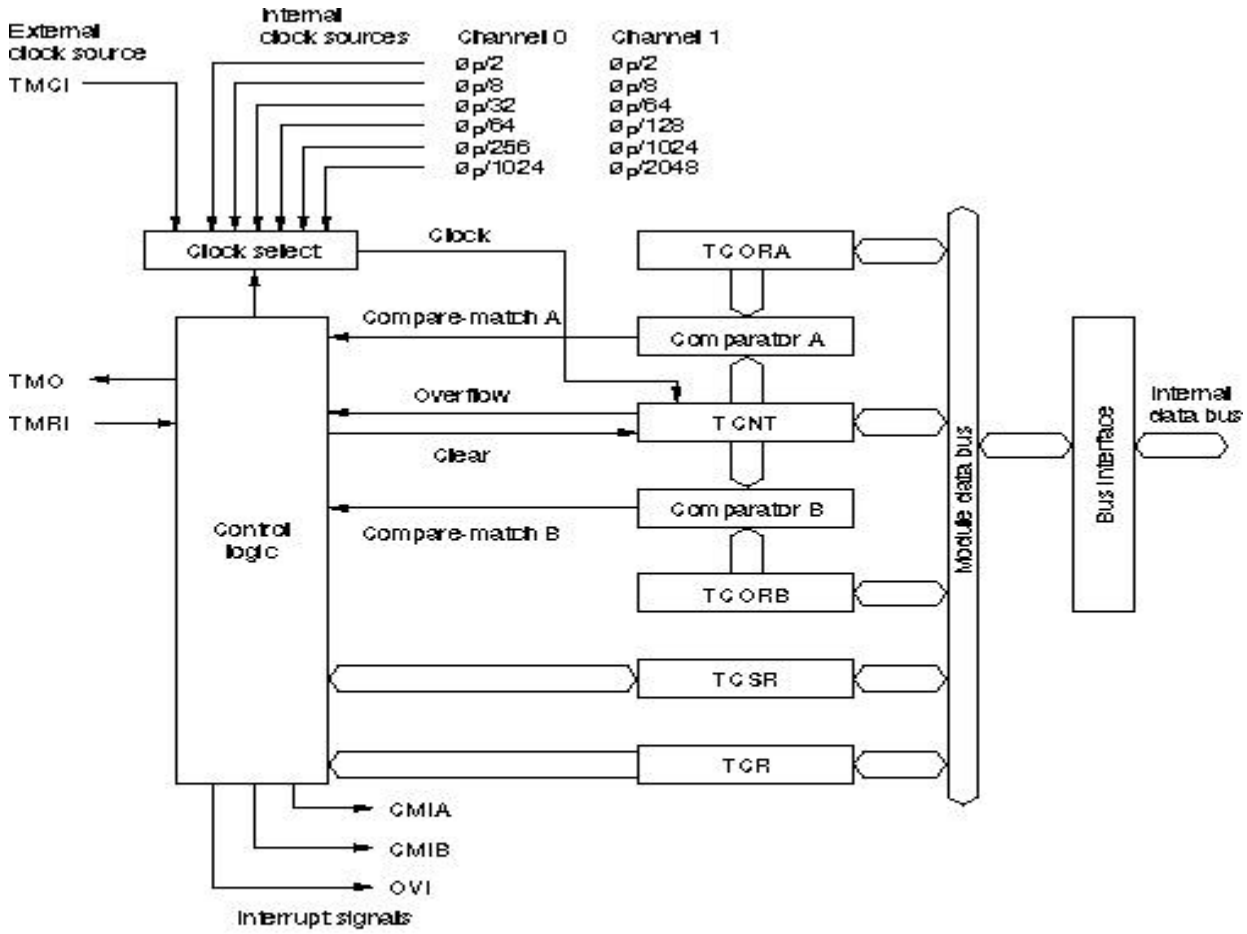
8-bit Timers (cont'd.)

Type Three (on both H8/300L and H8/300)

- Up to 2 channels
- Two independent comparators per channel - up to 2 PWM outputs controlled by compare-matches
- Counter clear options upon compare-match or external reset
- Selection of 7 clock options - 6 internal and 1 external
- Interrupt-generating capability - compare-match and/or overflow

8-bit Timer Block Diagram

Type 3 - H8/3437 one channel example



TCR: Timer control register (8 bits)
TCSR: Timer control status register (8 bits)
TCORA: Time constant register A (8 bits)
TCORB: Time constant register B (8 bits)
TCNT: Timer counter

PWM Timers

H8/300L

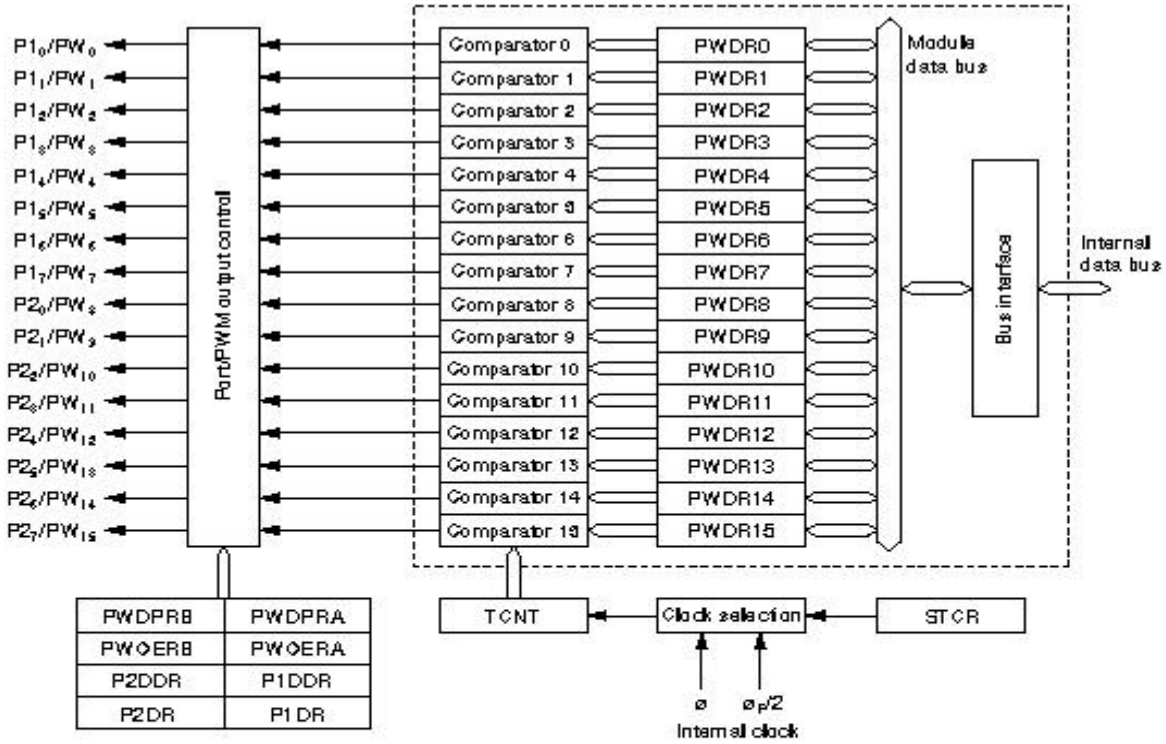
- Provides a PWM output with a variable dutycycle
- Offers 14-bit resolution
- Can be used as D/A converter with external low-pass filter

H8/300

- Provides 2 independent PWM outputs (except 16 for the H8/3217 and H8/3318 only)
  - generated by comparison between a single time base and up to 16 independent comparators
- Selection of up to 8 clock sources (internal or external)
- Signal control features
  - Direct or inverted PWM polarity output
  - Software enable/disable control

PWM Block Diagram

H8/3217 example



Legend

PWDR:	PWM data register
PWDPRA:	PWM data polarity register A
PWDPRB:	PWM data polarity register B
PWOERA:	PWM output enable register A
PWOERB:	PWM output enable register B
P1DDR:	Port 1 data direction register
P2DDR:	Port 2 data direction register
P1DR:	Port 1 data register
P2DR:	Port 2 data register
STCR:	Serial/timer control register

Watchdog Timer

Monitors system operation

- By resetting the CPU
- By generating an NMI (H8/300 only)

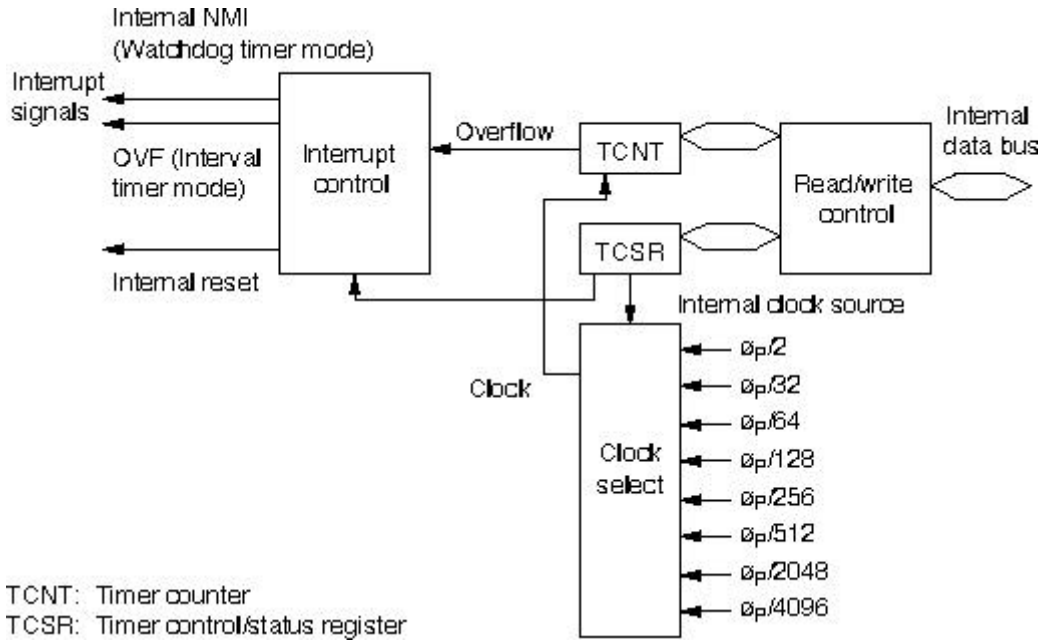
Selection of 8 clock sources

8-bit resolution

Can also operate as an interval timer

- Generates an interrupt at each overflow

Watchdog Timer Block Diagram
H8/3437 example



Serial Communication Interface (SCI)

Type 1 (only on H8/300L devices)

- One channel - operating synchronously ONLY
  - 8 or 16-bit data length
  - supports SSB (synchronized serial bus) communication with multiple devices on the H8/3644
  - interrupt generating capability - upon end of transfer
  - selectable internal or external clock sources

Type 2 (only on some H8/300L devices)

- One channel - operating synchronously ONLY
  - automatic transfer of up to 32 bytes of data
    - » transfer can be triggered externally
    - » strobe pulse can be output per each transfer
    - » delays can be inserted between each transfer
  - selectable internal or external clock sources
  - interrupt generating capability - end of transfer or error

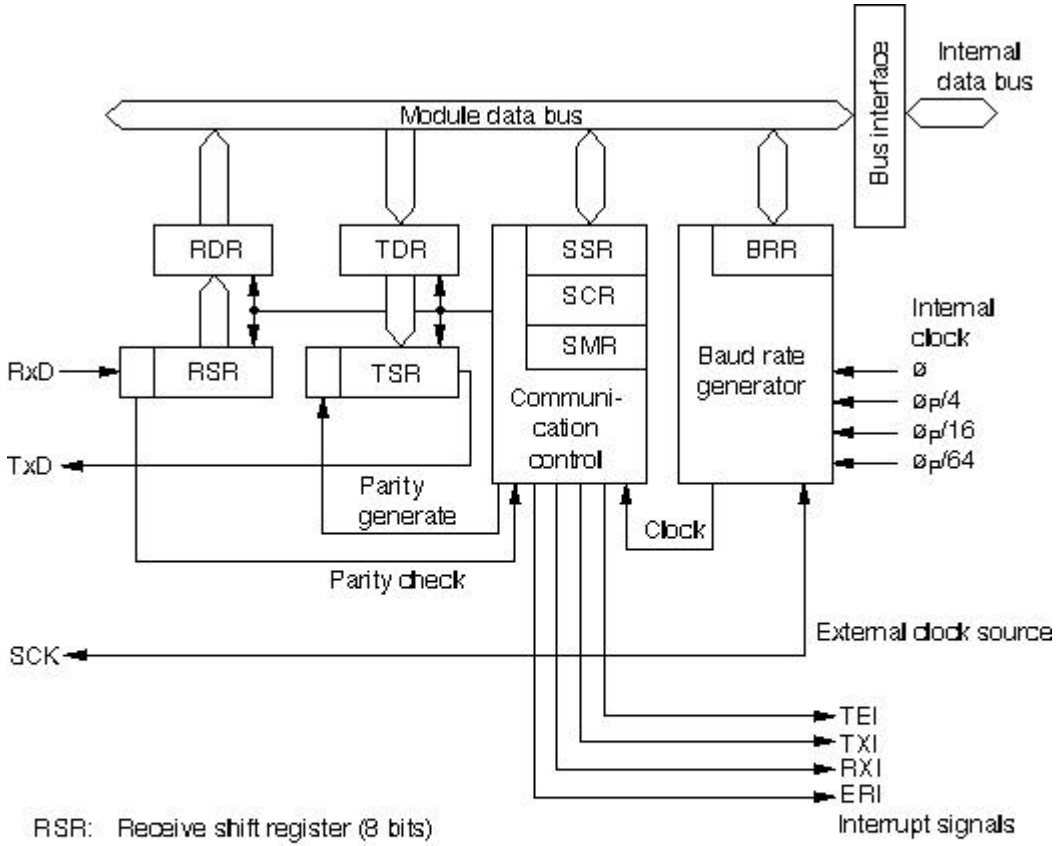
SCI (cont'd.)

Type 3 (all except some H8/300L devices)

- Up to 2 channels (one channel on H8/300L)
- Asynchronous operation
  - adheres to standard asynchronous communication formats
  - error-checking and break detection capabilities
  - max. 156K bits/sec. **(H8/300L),** max. 500Kbits/sec. **(H8/300)**
- Synchronous operation
  - 8-bit data length
  - max. 2.5Mbits/sec. **(H8/300L),** max. 4Mbits/sec. **(H8/300)**
- Full duplex communication
- Built-in baud rate generator - selectable bit rates
- Selectable clock sources - internal or external
- Interrupts upon end of transmission/receive and/or communication error
- Multiprocessor function **(H8/300 only)**
  - serial communication with multiple devices

SCI Type 3 Block Diagram

H8/3437 - one channel example



RSR: Receive shift register (8 bits)
RDR: Receive data register (8 bits)
TSR: Transmit shift register (8 bits)
TDR: Transmit data register (8 bits)
SMR: Serial mode register (8 bits)
SCR: Serial control register (8 bits)
SSR: Serial status register (8 bits)
BRR: Bit rate register (8 bits)

I^2C Interface

Provided on some H8/300 devices only

Subset of the Philips I^2C serial bus interface protocol

Up to 2 channels of 2-wire serial link between H8 and peripheral devices

- Comprises a single data line and a clock line

Operation features

- Master/slave receive and transmit mode support
- Automatic generation of start/stop conditions
- Wait state insertion during acknowledgement mode

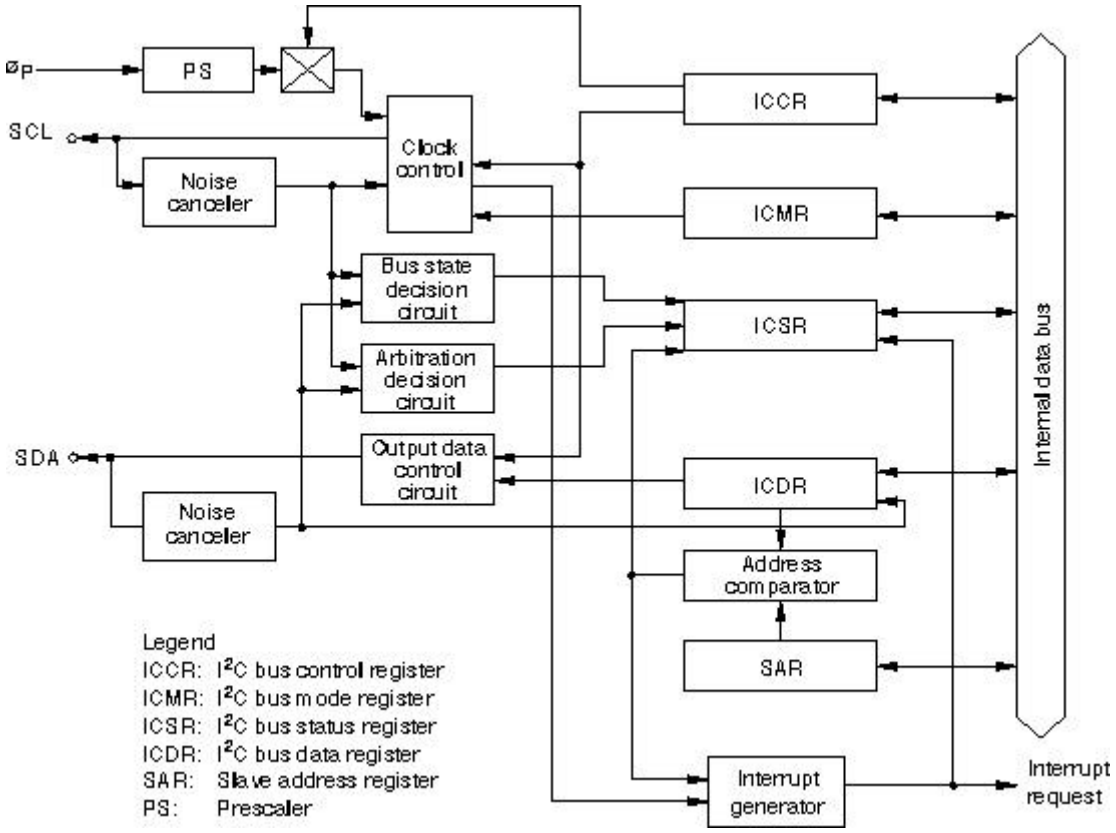
Selection of 8 internal clock sources (master mode)

Three interrupt sources

- Data transfer end
- Slave address match (in slave receive mode)
- Bus arbitration lost (in master transmit mode)

I²C Block Diagram

H8/3437 example



A/D Converter

Up to twelve separate input channels (H8/38XX, else eight)

Up to 10-bit resolution (8-bit on H8/300L)

Sample-and-hold function

Up to 2 conversion modes

- Single mode: one channel A/D conversion
- Scan mode: up to 4 channel sequential conversion **(H8/300 ONLY)**

Conversion speed

- Max. 124µs, min. 12.4µs **(H8/300L)**, max. 8.4µs **(H8/300)**

Trigger mechanisms

- By software or by dedicated input pin

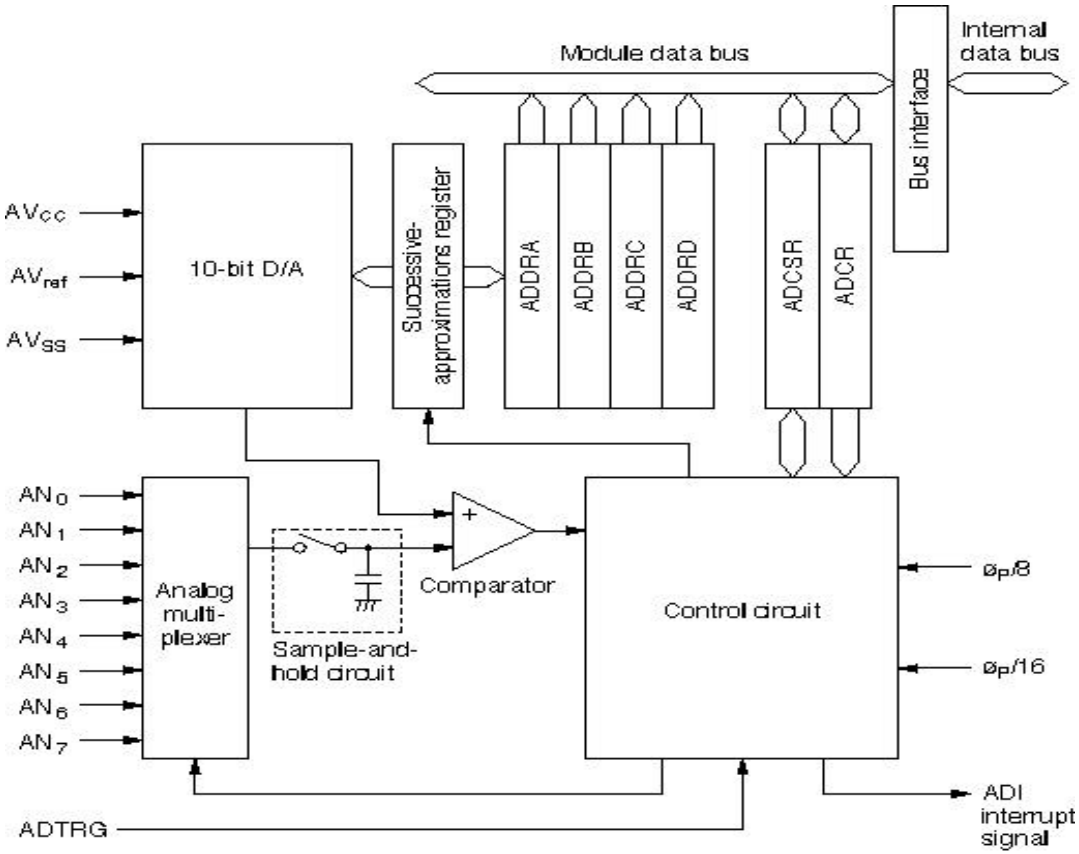
Interrupt generating capability

- Upon end of conversion

Selectable analog conversion voltage range (H8/300 only)

A/D Block Diagram

H8/3437 example



Legend
ADCR: A/D control register
ADCSR: A/D control/status register
ADDRA: A/D data register A
ADDRB: A/D data register B
ADDRC: A/D data register C
ADDRD: A/D data register D

D/A Converter

- Only on H8/300
- Two independent channels
- 8-bit resolution
- Conversion time - max 10ms
- Selectable output voltage range

Liquid Crystal Display (LCD) Controller

Only on some H8/300L (H8/38xx)

Up to 40 segment on-chip display driving capability

- Up to 512 segments when used with external driver

LCD RAM capacity of 512 bits (8 bits x 64 bytes)

- Word access capacity

Internal voltage divider

- Provided to LCD power supply

Unused common lines can be used to boost common output

Displays in all operation modes (except standby)

Host Interface Controller (HIF)

Provided on some H8/300 (IKAP*) devices only

Dual-channel 8-bit parallel interface between CPU and host processor (e.g. Intel 80x86 devices)

- H8 is slaved to the host processor

Communication protocol consists of

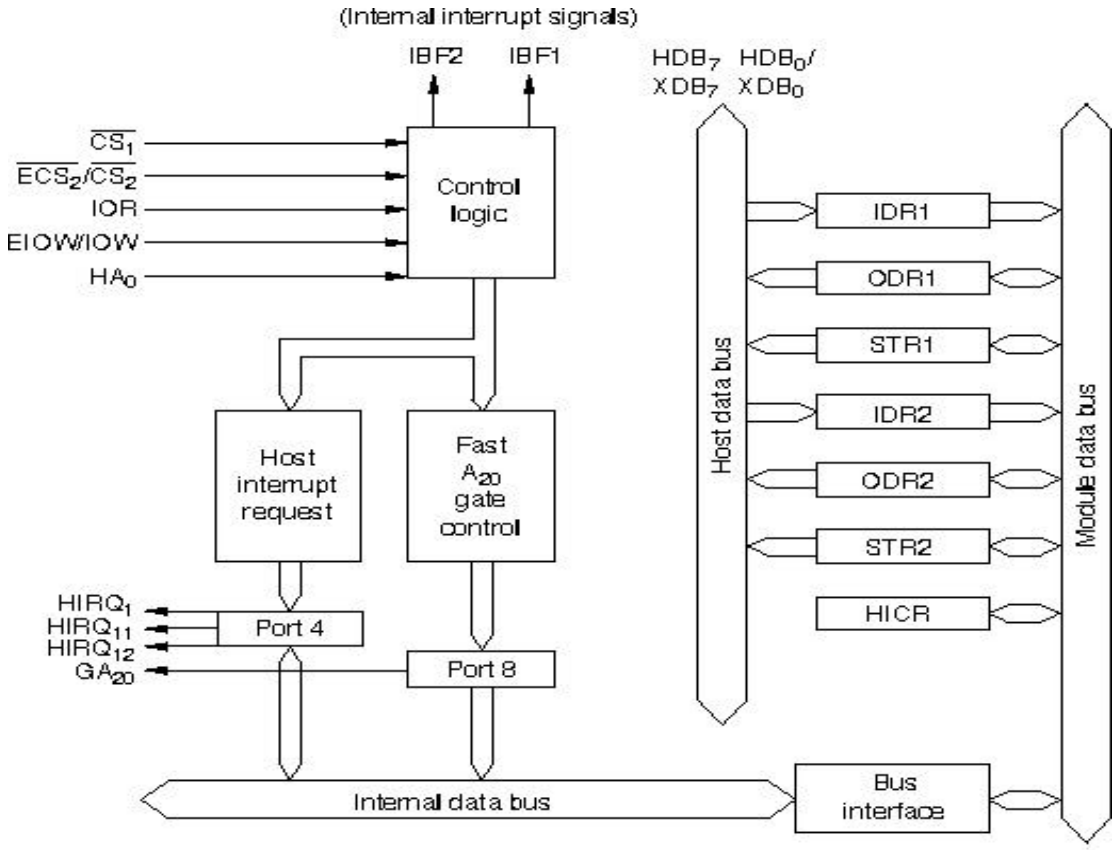
- Control signals from the host processor to the H8 CPU (e.g. chip selects, read/write signals, address select)
- Output signals from H8 CPU to the host processor (A20 gate signal, interrupt requests to host)
- 8-bit bi-directional command/data bus

Two operation types (both emulate an addressing mode used by Intel 80x86-powered PCs):

- Regular host interface operation
- Fast GATE A20 operation

***IKAP = Intelligent KeyBoard And Power management (H8/333X, 343X, & 321X)**

HIF Block Diagram
H8/3437 example



Legend
IDR1: Input data register 1
IDR2: Input data register 2
ODR1: Output data register 1
ODR2: Output data register 2
STR1: Status register 1
STR2: Status register 2
HICR: Host interface control register

Keyboard Controller Function

Provided on some H8/300 (IKAP*) devices only

Provides a key-sense interrupt function scheme

- Controls a matrix keyboard using a keyboard scan with wake-up interrupt and sense port configuration

Used for keyboard control of an Intel 80x86-based laptop

- H8 CPU operates in the host interface slave mode

BIOS firmware support provided by SystemSoft and Phoenix Technologies

***IKAP = Intelligent KeyBoard And Power management (H8/333X, 343X, & 321X**

Interrupt Processing

Two types

- External interrupts
  - maskable IRQs - up to 13 **(H8/300L)** and 9 **(H8/300)**
  - NMI - only on **H8/300**
  - sensed upon rising or falling edge
- Internal interrupts (from on-chip modules e.g. SCI, timers, A/D, etc.)
  - up to 21 **(H8/300L)** and 33 **(H8/300)**

Masking vs. enabling

- All interrupts (except NMI) can be masked
- All interrupts can be individually enabled

Individually vectored - automatic interrupt handling

Interrupts prioritized in the vector table

16-bit CISC Peripherals

- H8/300H and H8S
- Interrupt Processing

16-bit CISC Peripheral Modules

Modules	H8/300H	H8S/21xx	H8S/22xx-H8S/26xx
Bus Controller	✓	✓	✓
Timer Unit (ITU or TPU)	✓	-	✓
Pattern Generator (TPC or PPG)	✓	-	✓
16-bit Free Running Timer	-	✓	-
8-bit General-Purpose Timers	-	✓	-
PWMs	-	✓	-
DMA Controller	✓	-	✓
Data Transfer Controller (DTC)	-	✓	✓
Serial Communication Interface (SCI)	✓	✓	✓
I^2C Interface	-	✓	-
A/D Converter	✓	✓	✓
D/A Converter	✓	✓	✓

Bus Controller

Partitions memory space into 8 distinct blocks

Provides chip select lines for each memory block

Selects access data size as 8-bit or 16-bit for each block

Selects access cycles as 2 or 3-state for each block

Inserts wait states (by software, hardware, or both)

Provides bus arbitration and prioritization

- CPU < DMAC < Refresh Controller < External Bus Master

Additional features - H8/3067, H8S/22xx-26xx only

- Idle cycle insertion - to avoid bus timing problems
- Write buffer functions - for parallel task execution

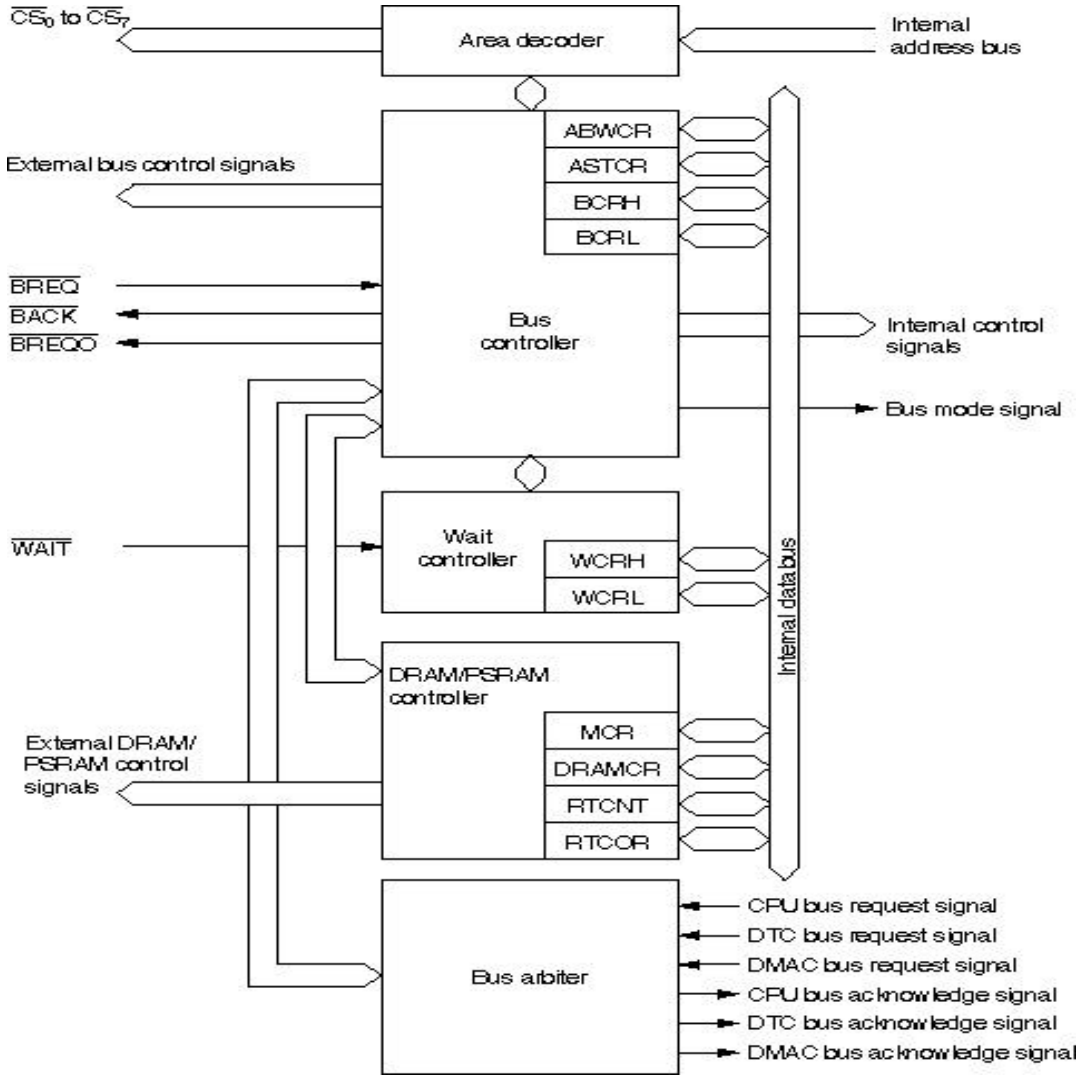
Bus Controller (cont'd.)

External memory support

- Glueless DRAM interface capability
  - up to 8Mbyte (64Mbit DRAM bank)
  - provides RAS, 2CAS or 2WE access signals
  - row address/column address multiplexed output (8/9/10 bits)
  - fast page mode support **(H8/3067 and H8S/22xx-26xx)**
  - CAS-before-RAS or self refresh options
- Glueless Burst ROM interface capability **(H8/3067 and H8S/22xx-26xx)**
  - up to 2Mbyte support
- PSRAM interface support
- Direct SRAM/EPROM connectivity

Bus Controller Block Diagram

H8S/2655 example



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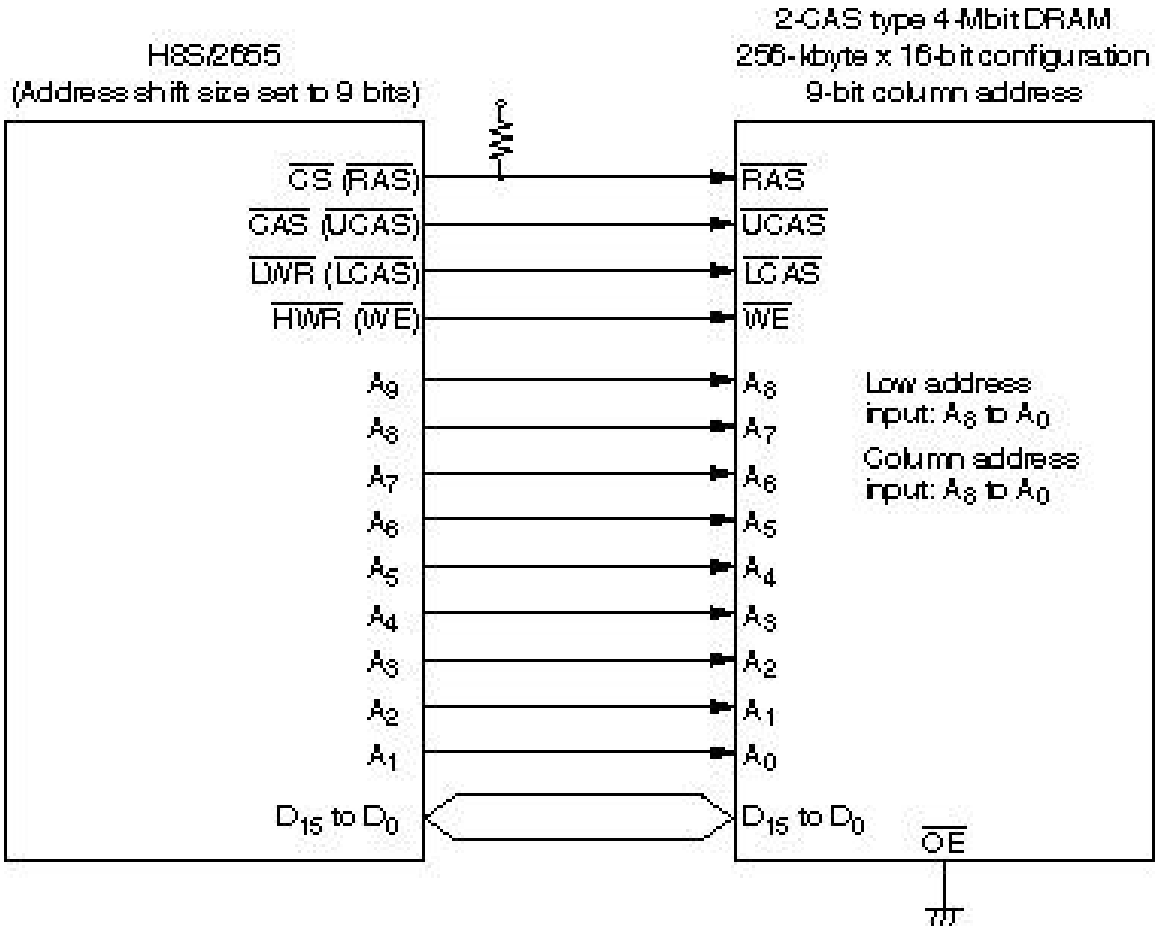
DRAM Connection Example
H8S/2655



Timer Unit (ITU or TPU)*

Up to 6 16-bit channels (5 on some H8/300H)

- Two comparators/input-capture registers and a timer counter per channel
- Free-running, periodic, or external event counter operation options

Selection of 8 clock sources (internal or external)

Buffering

- Input-capture registers in up to 4 channels

Interrupt-generating capability

- Up to 26 sources (compare-match, input-capture, overflow, underflow)
- Can activate DMA transfers upon compare-match/input-capture
- Can trigger pattern generator module to produce up to 16 PWM outputs
- Compare-match/input-capture can be used to start A/D conversion

*** ITU = Integrated Timer Unit (H8/300H)**
TPU = Timer Pulse Unit (H8S/22xx-26xx)

ITU/TPU (cont'd.)

Operation Modes

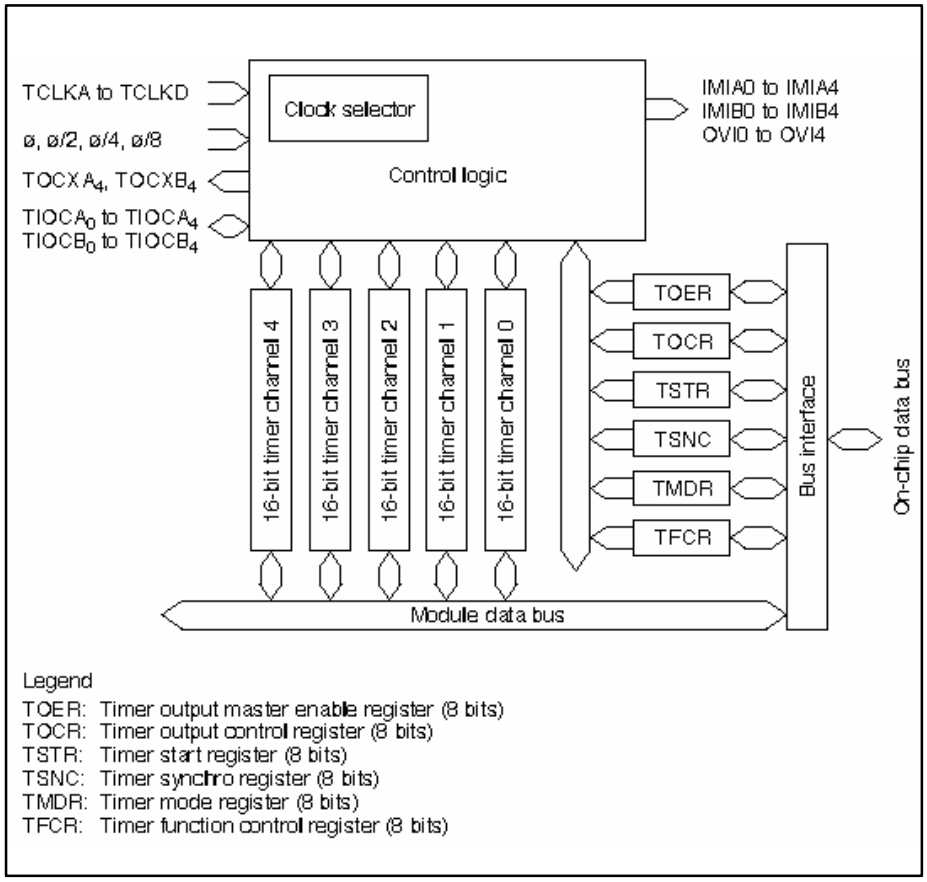
- Normal operation
  - up to 16 simultaneous toggle/compare-match outputs
  - up to 16 capture inputs
  - one-shot output capability
- Synchronous operation
  - 2 or more counters can be preset or cleared simultaneously
- PWM modes
  - selectable duty-cycle
  - up to 15-phase PWM output possible
  - complementary overlapping or non-overlapping combinations possible
- Phase-counting mode
  - calculates phase difference between 2 external square-wave inputs

Cascaded operation (H8S/22xx-26xx only)

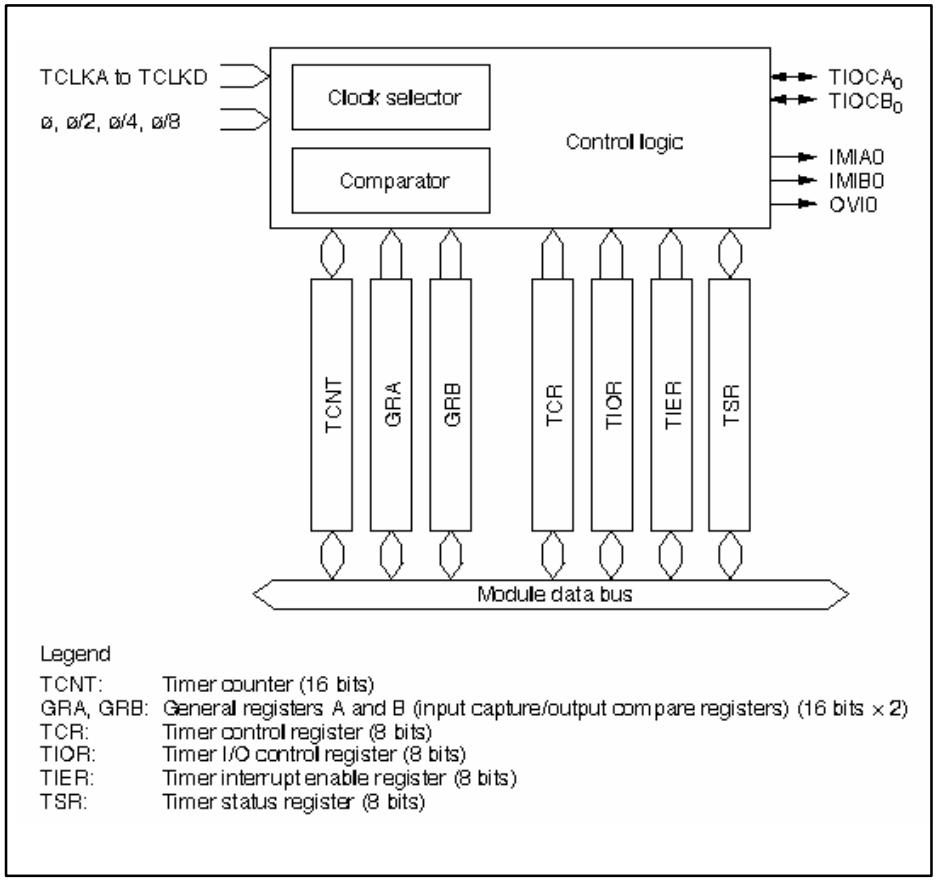
- 2 16-bit channels combined operate as 32-bit timer

ITU Block Diagram

H8/3048 - example



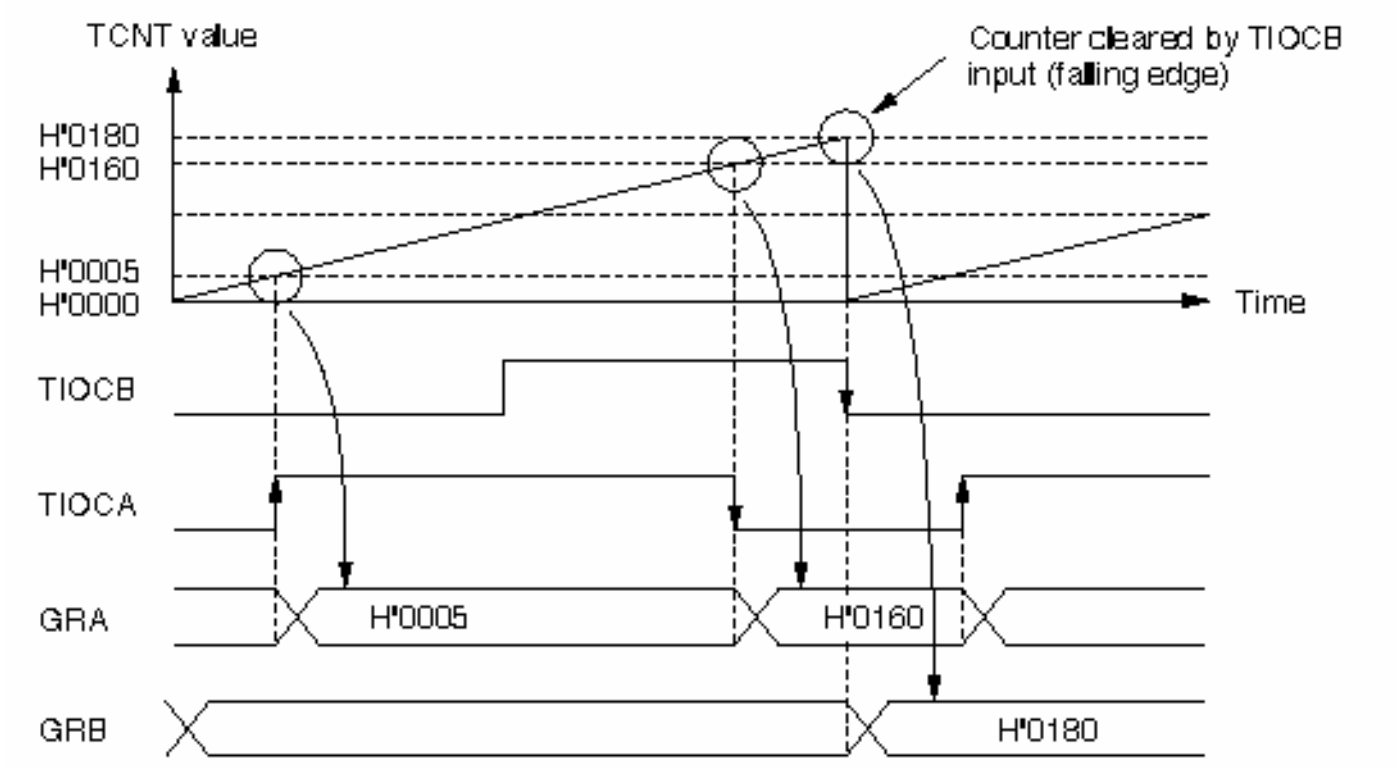
ITU overall block diagram



ITU channel 0 block diagram

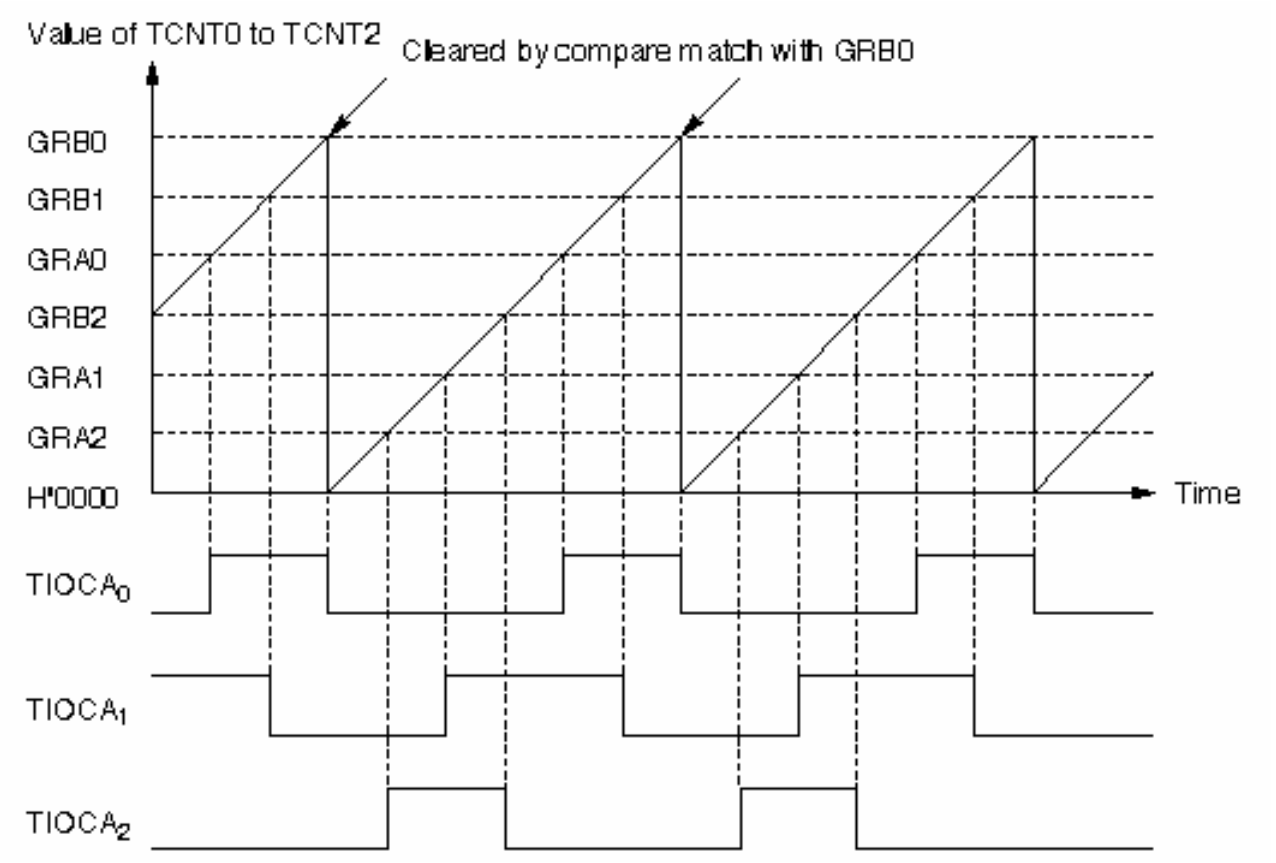
ITU/TPU Operation Example

H8/3048 - Input Capture



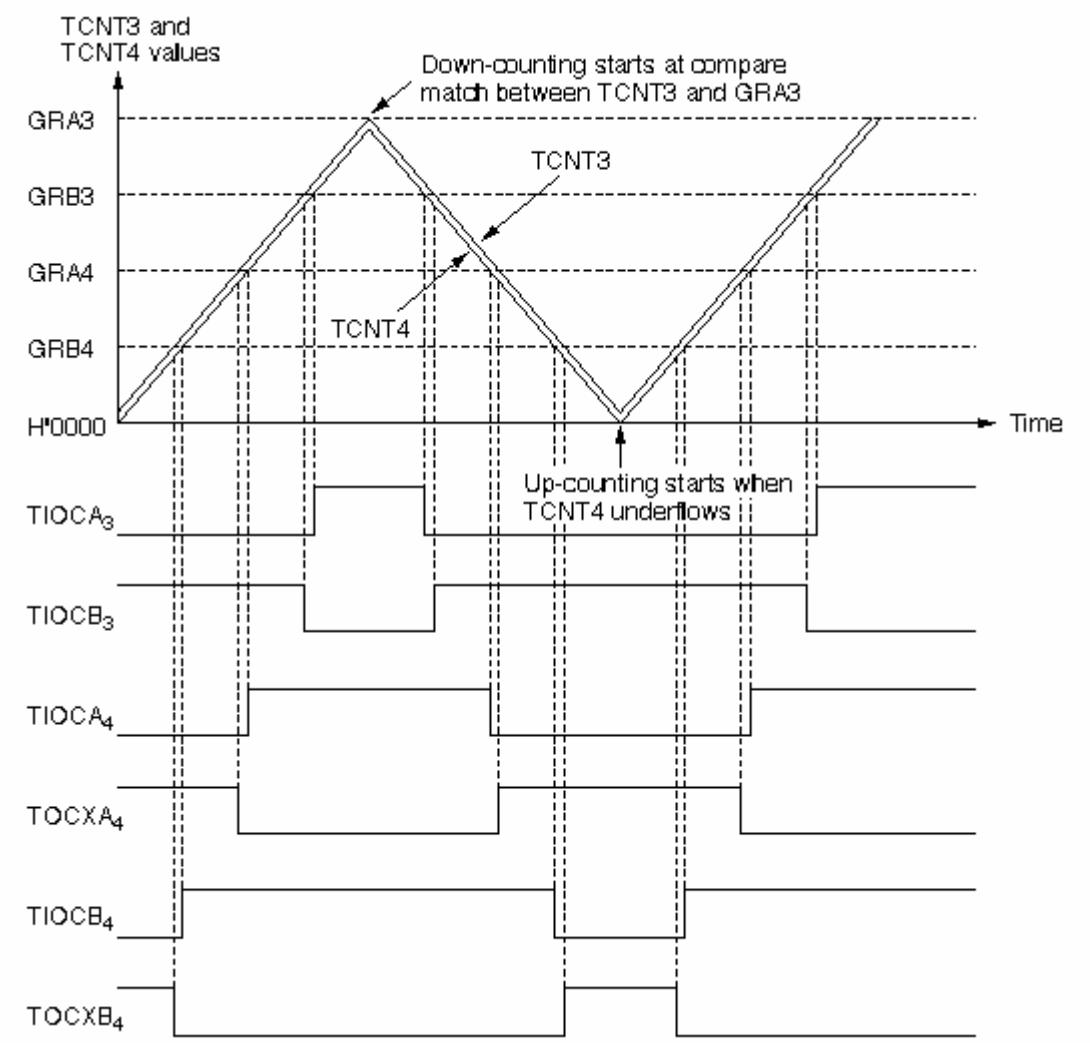
ITU/TPU Operation Example

H8/3048 - Synchronized Operation



ITU/TPU Operation Example

H8/3048 - Complementary PWM Mode



Pattern Generator (TPC or PPG*)

Outputs up to 16 independent PWM waveforms

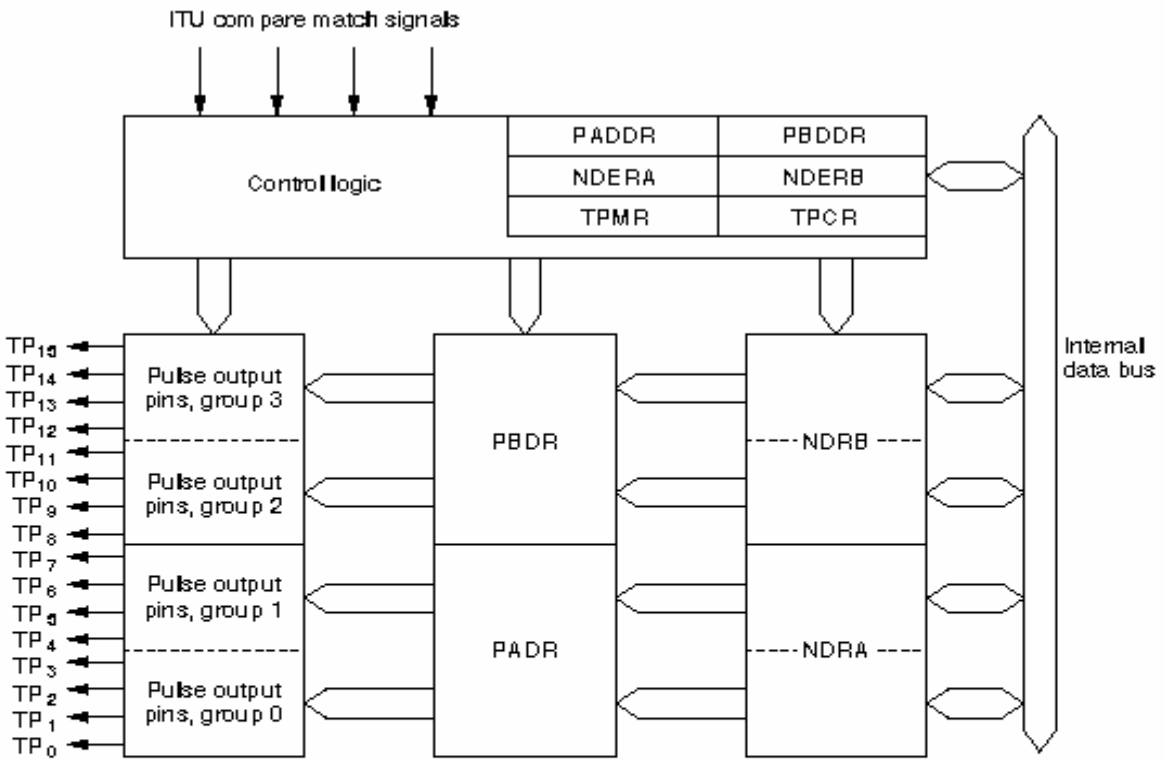
Trigger mechanism

- Compare-match from 4 ITU channels
- Trigger signals activate groups of 4 outputs at a time
- Overlapping or non-overlapping output options
- Can operate in conjunction with the DMAC
  - Compare-match trigger signals can activate the DMAC for sequential transfer of output pattern to the TPC

*** TPC = Timing Pattern Controller (H8/300H)**
PPG = Programmable Pattern Generator (H8S/22xx-26xx)

TPC/PPG Block Diagram

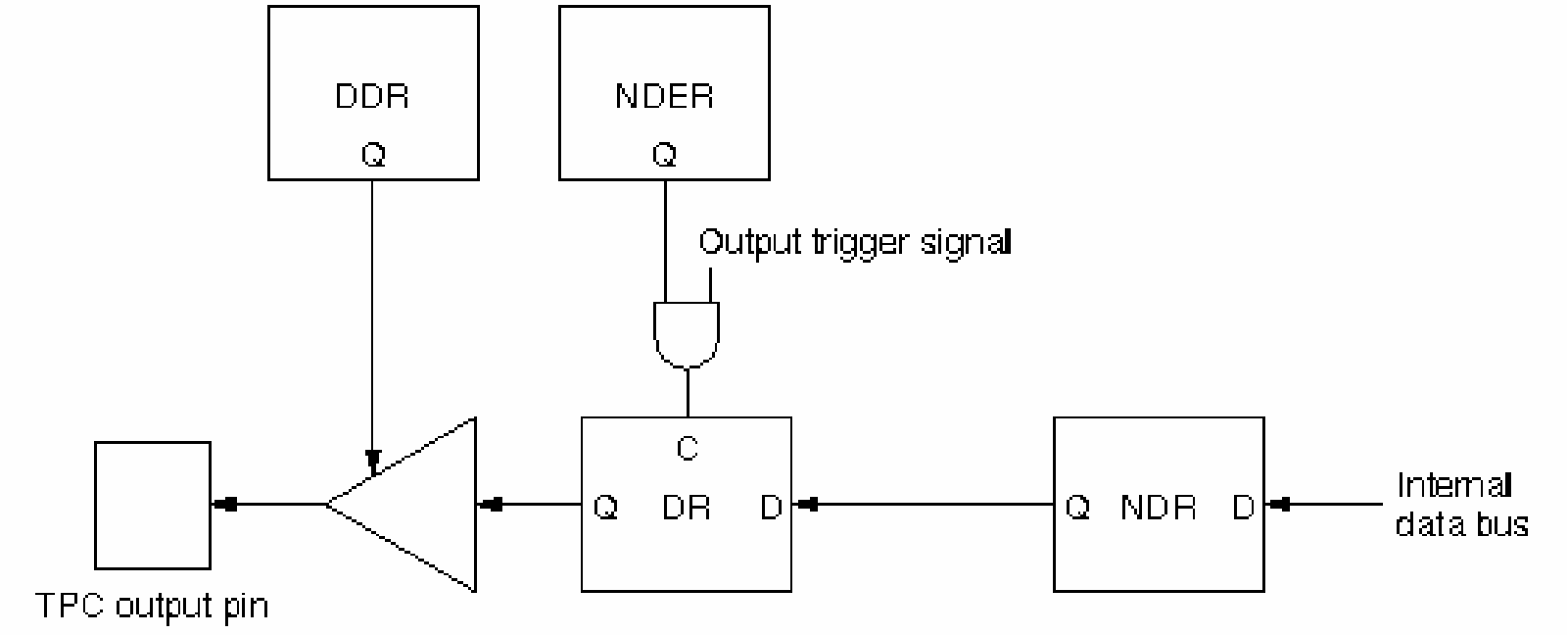
H8/3048 example



Legend
TPMR: TPC output mode register
TPCR: TPC output control register
NDERB: Next data enable register B
NDERA: Next data enable register A
PBDDR: Port B data direction register
PADDR: Port A data direction register
NDRB: Next data register B
NDRA: Next data register A
PBDR: Port B data register
PADR: Port A data register

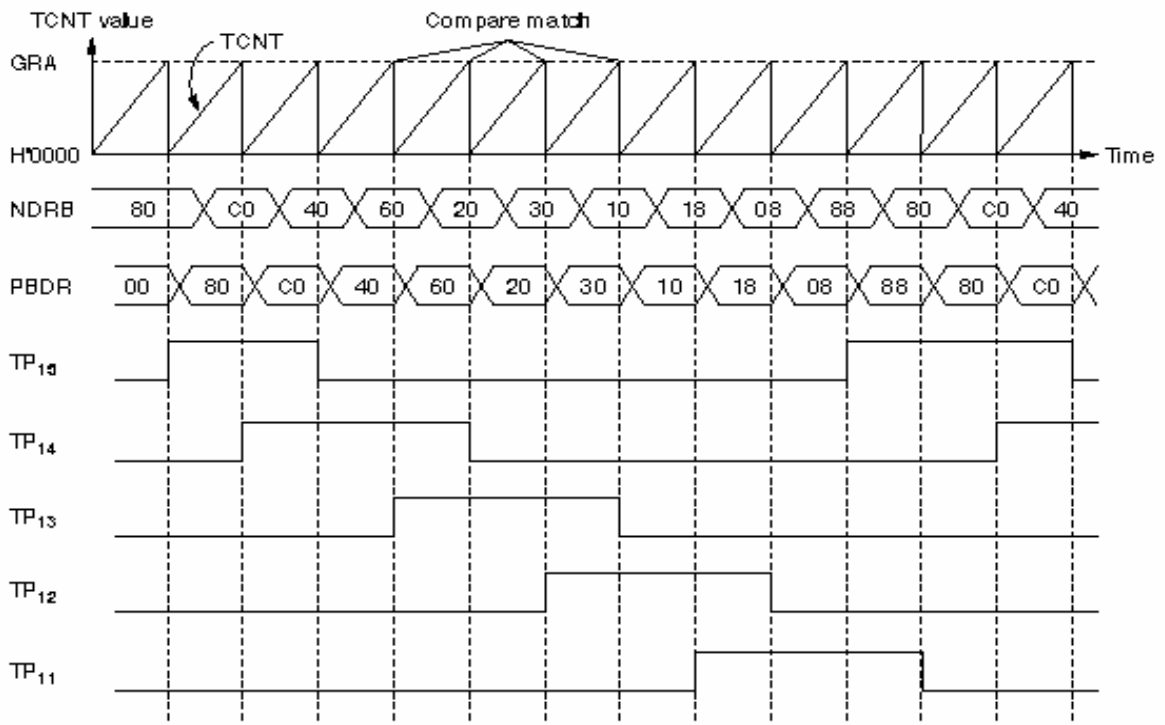
TPC/PPG Operation

H8/3048 example



TPC/PPG Operation Example

H8/3048 - 5 PWM output pattern



- The ITU channel to be used as the output trigger channel is set up so that GRA is an output compare register and the counter will be cleared by compare match A. The trigger period is set in GRA. The IMIEA bit is set to 1 in TIER to enable the compare match A interrupt.
- H'F8 is written in PBDDR and NDERB, and bits G3CMS1, G3CMS0, G2CMS1, and G2CMS0 are set in TPCR to select compare match in the ITU channel set up in step 1 as the output trigger. Output data H'80 is written in NDRB.
- The timer counter in this ITU channel is started. When compare match A occurs, the NDRB contents are transferred to PBDR and output. The compare match/input capture A (IMFA) interrupt service routine writes the next output data (H'C0) in NDRB.
- Five-phase overlapping pulse output (one or two phases active at a time) can be obtained by writing H'40, H'60, H'20, H'30, H'10, H'18, H'08, H'88... at successive IMFA interrupts. If the DMAC is set for activation by this interrupt, pulse output can be obtained without loading the CPU.

16-bit Free Running Timer (FRT)

Only on H8S/21xx devices

One channel with 2 independent comparators

- Up to 2 simultaneous waveforms

Four input-capture lines

- Current count can be captured on rising/falling edge of input signal
- Two channels can be used as buffers for the other 2 channels

Counter clear option - upon compare-match

Selection of 4 clock options

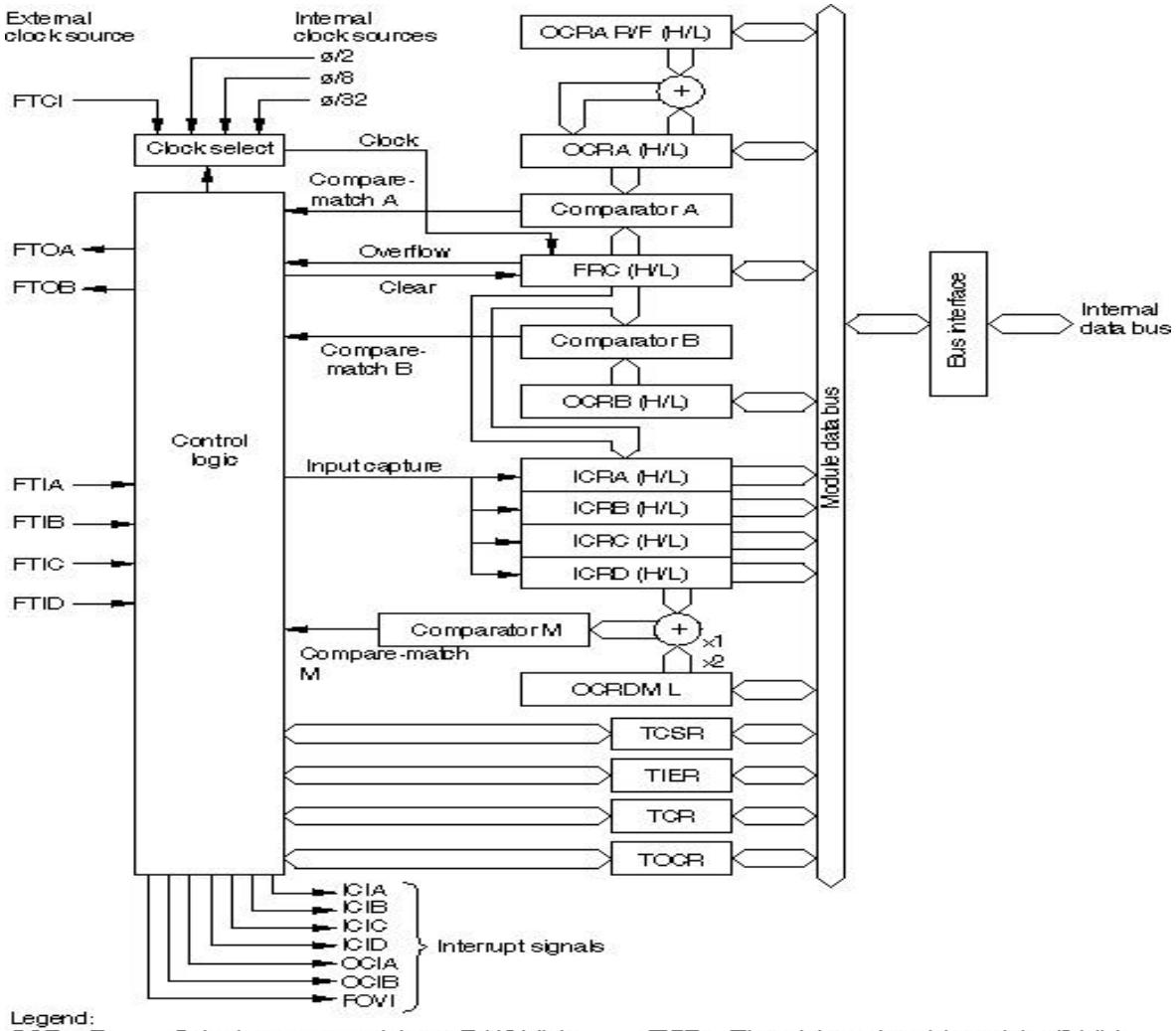
- 3 internal and 1 external

Interrupt-generating capability

- 7 interrupts upon compare-match, input-capture, and/or overflow

FRT Block Diagram

H8S/2144 example



Legend:

OCRA, B:	Output compare register A, B (16 bits)	TIER:	Timer interrupt enable register (8 bits)
FRC:	Free-running counter (16 bits)	TCR:	Timer control register (8 bits)
ICRA, B, C, D:	Input capture register A, B, C, D (16 bits)	TOCR:	Timer output compare control register (8 bits)
TCSR:	Timer control/status register (8 bits)		

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8-bit General Purpose Timers

Only on H8S/21xx devices

Up to 2 channels

- Two independent comparators per channel - up to 2 PWM outputs controlled by compare-matches

Counter cleared upon compare-match or external reset

Selection of up to 7 clock options

- Six internal and one external

Interrupt-generating capability

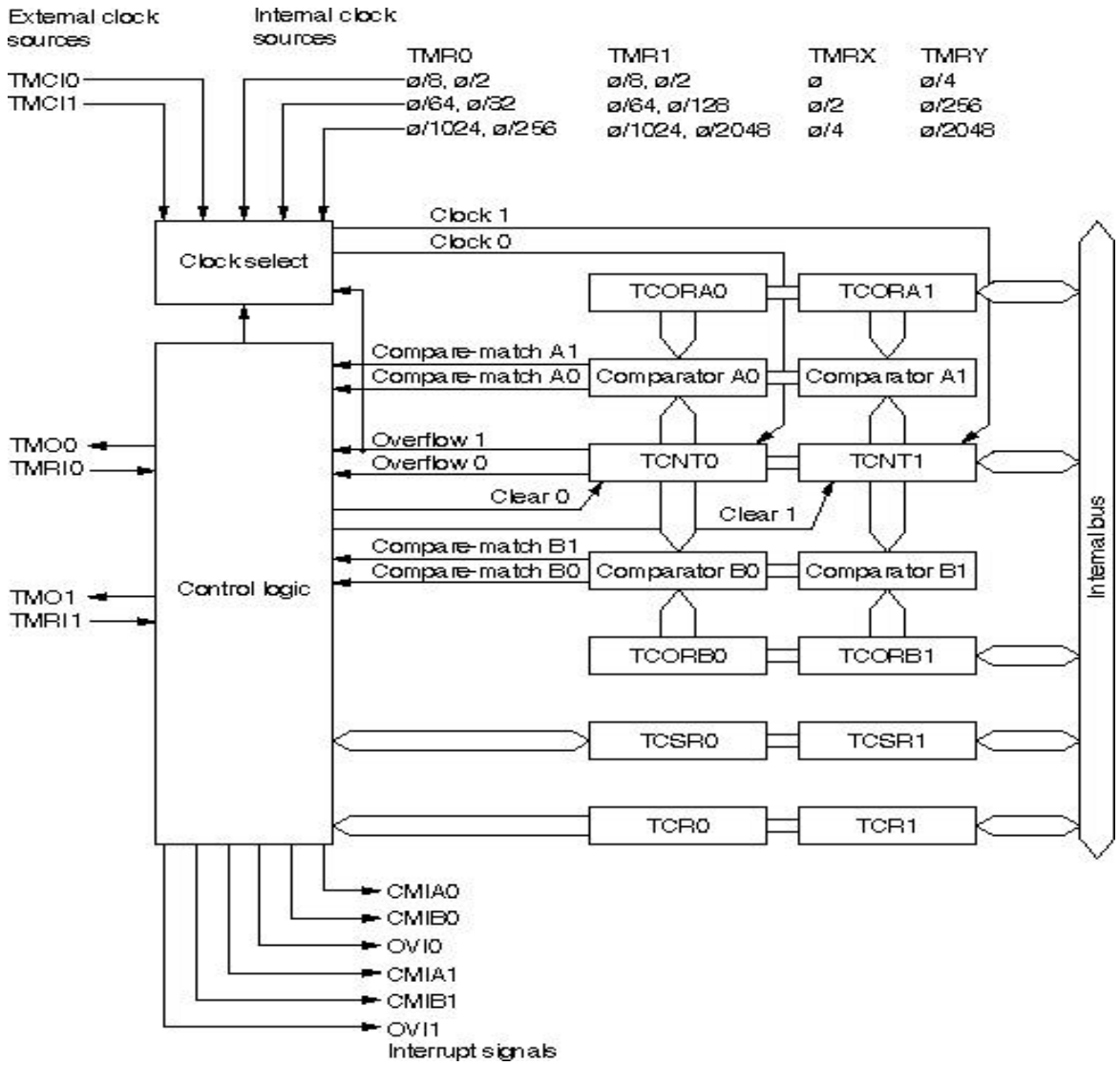
- Compare-match and/or overflow

Cascade operation

- Channels can be linked to operate as 16-bit timer

8-bit Timers Block Diagram

H8S/2144 example



PWM Timers
Only on H8S/21xx devices

8-bit PWM Timer

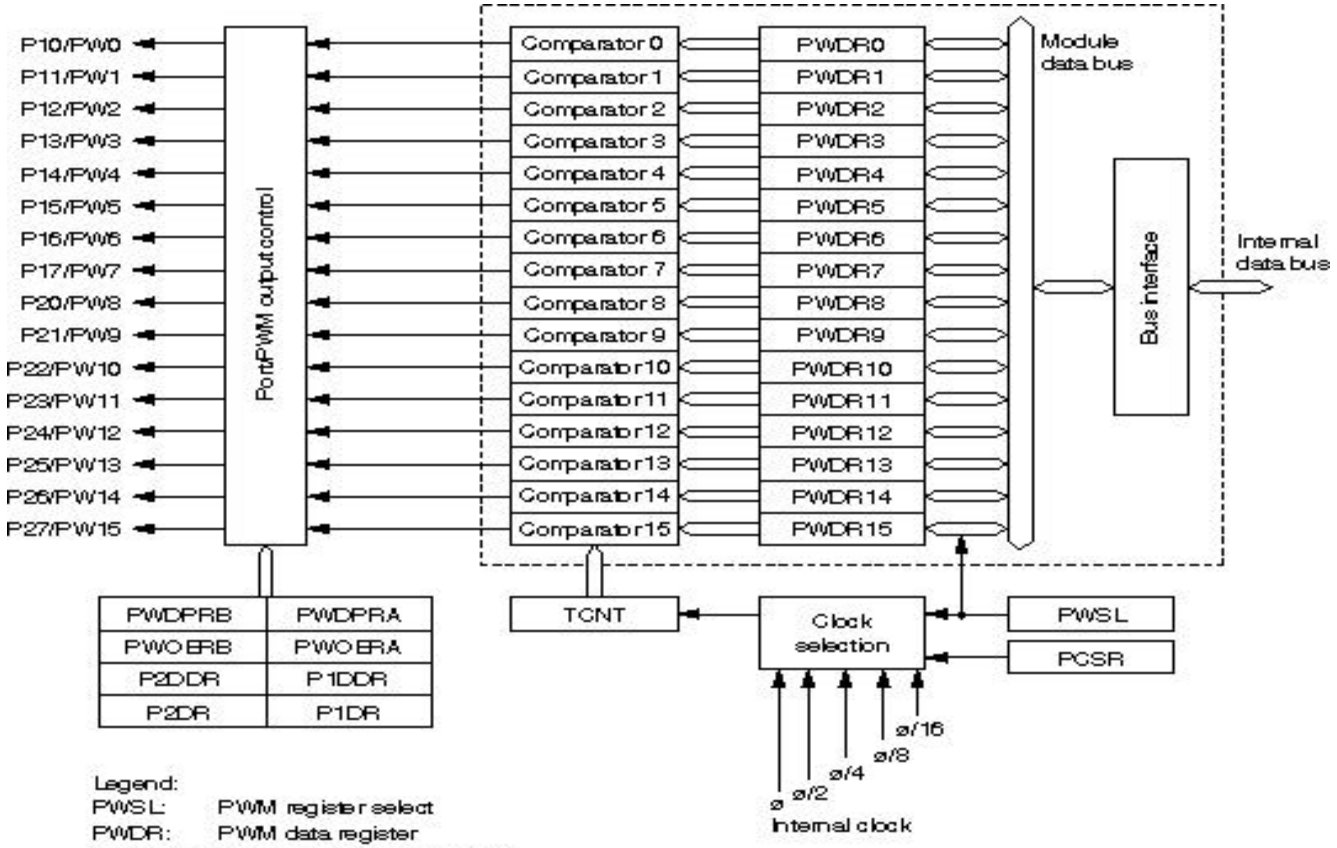
- Provides 16 independent PWM outputs
  - generated by comparison between one time base and 16 independent comparators
  - adjustable duty cycle (0-100%)
  - max. 1.25MHz carrier frequency
  - direct or inverted outputs and enable/disable control
- Selection of 5 internal clock sources

14-bit PWM

- Provides 2 PWM outputs with a variable dutycycle
- Can be used as a 14-bit D/A converter if connected to external low-pass filter

8-bit PWM Block Diagram

H8S/2144 example



Legend:

PWSL:	PWM register select
PWDR:	PWM data register
PWDPRA:	PWM data polarity register A
PWDPRB:	PWM data polarity register B
PWOERA:	PWM output enable register A
PWOERB:	PWM output enable register B
PCSR:	Peripheral clock select register
P1DDR:	Port 1 data direction register
P2DDR:	Port 2 data direction register
P1DR:	Port 1 data register
P2DR:	Port 2 data register

Direct Memory Access Controller (DMAC)

Full address space can be specified

Byte/Word transfer options

Operation modes

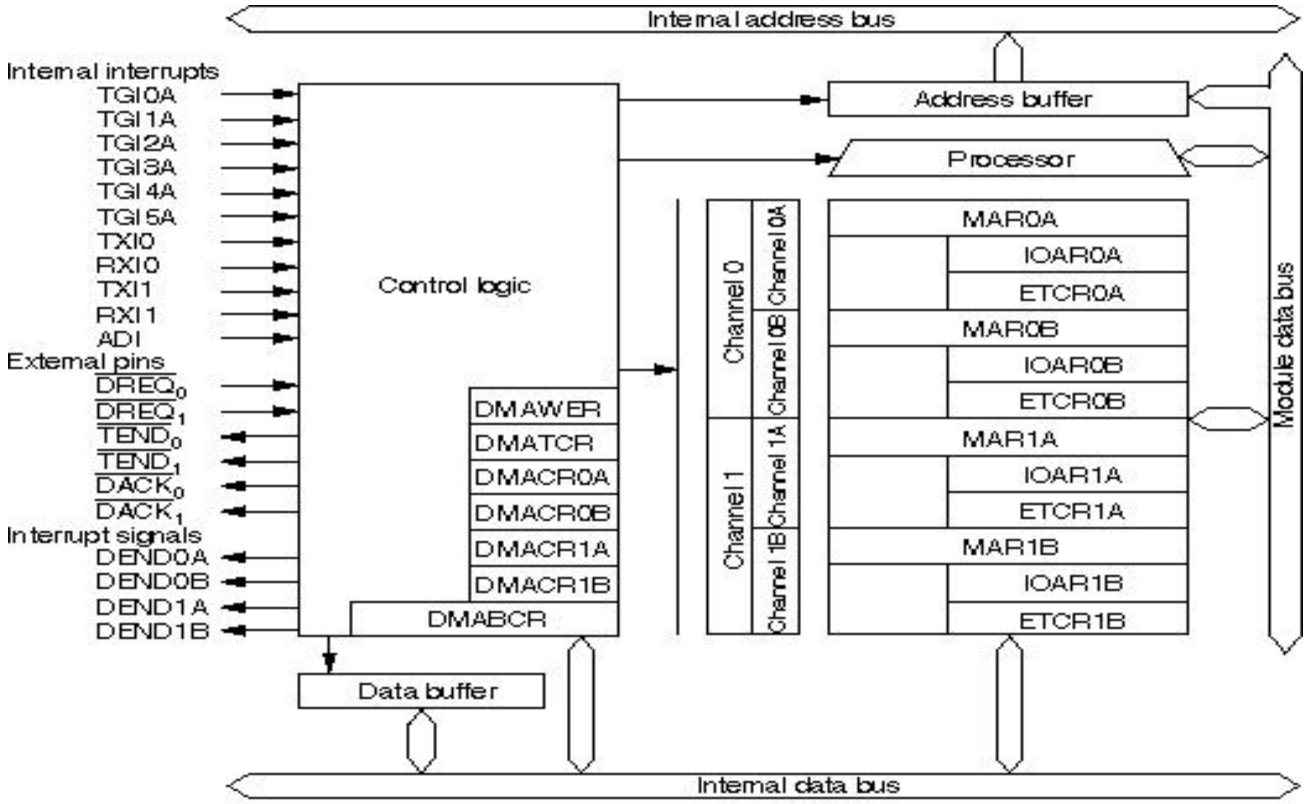
- Short address mode
- Full address mode

Activation sources

- Internal interrupts
  - upon timer compare-match/input-capture events
  - upon serial channel transmit/receive completion
  - upon A/D end-of-conversion (some devices only)
- External request
- Software request (auto-request)

DMAC Block Diagram

H8S/2655 example



Legend

DMAWER : DMA write enable register
DMATCR : DMA terminal control register
DMABCR : DMA band control register (for all channels)
DMACR : DMA control register
MAR : Memory address register
IOAR : I/O address register
ETCR : Executive transfer counter register

DMAC Modes of Operation

Single address (fly-by) operation - only on H8S/22xx-26xx

- Single cycle bus transfer
- Maximum 4 channels

Other short address modes

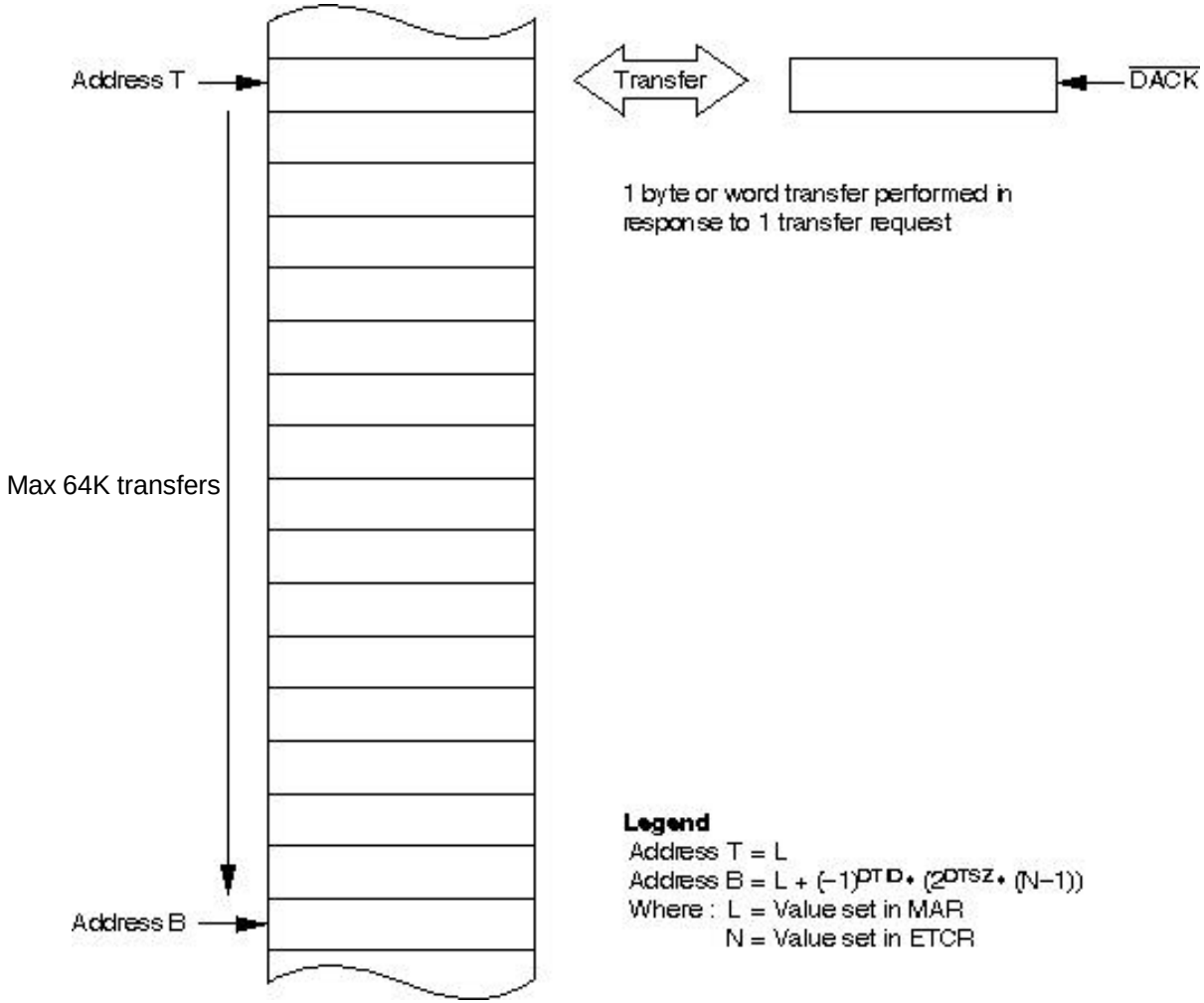
- Sequential (I/O) mode
- Idle mode
- Repeat mode
- 4 channel simultaneous operation (8 channels on H8/3003)

Full address

- Normal transfer operation
- Block transfer operation
- 2 channel simultaneous operation (4 channels on H8/3003)

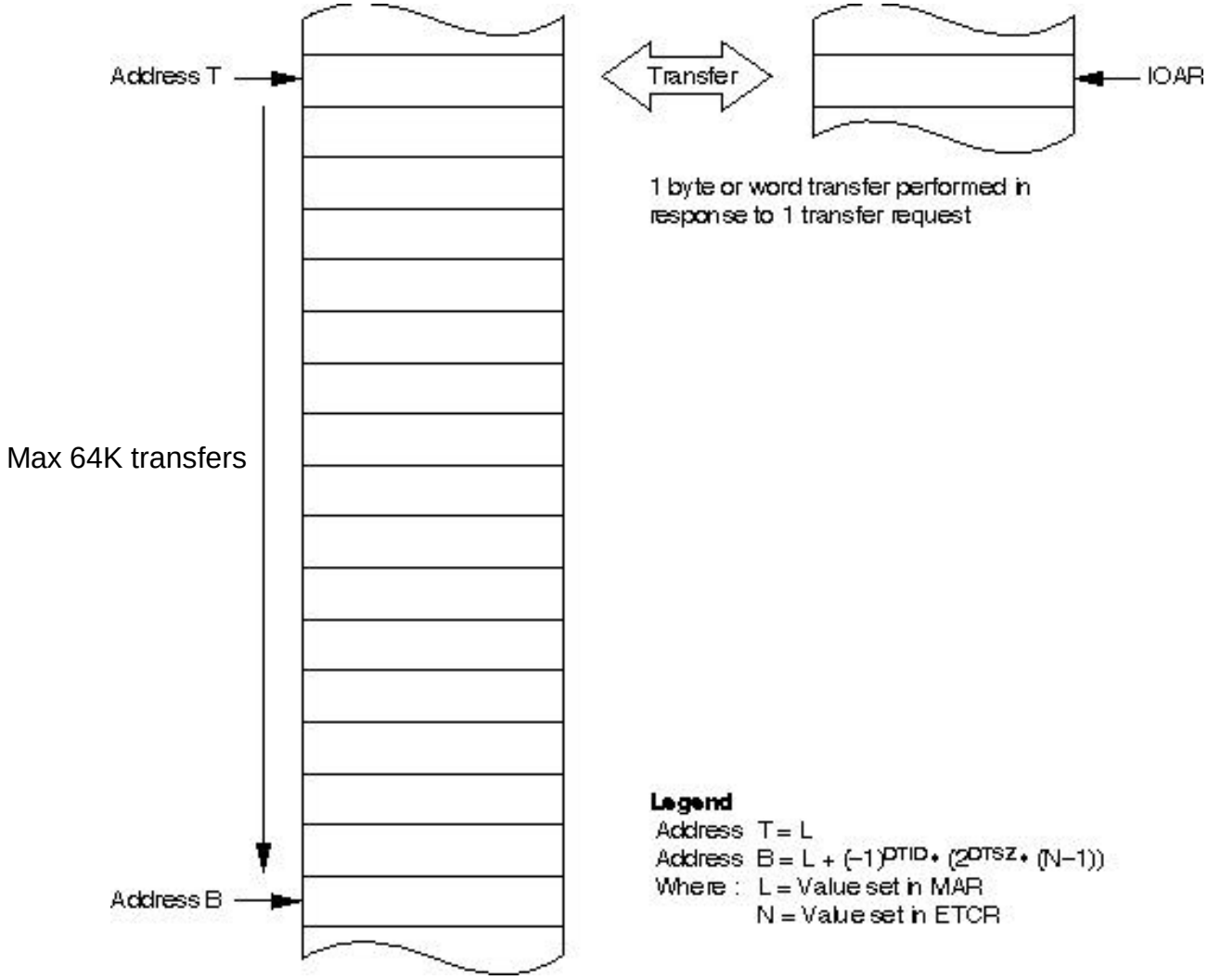
DMAC Single Address Mode Operation

H8S/2655 example

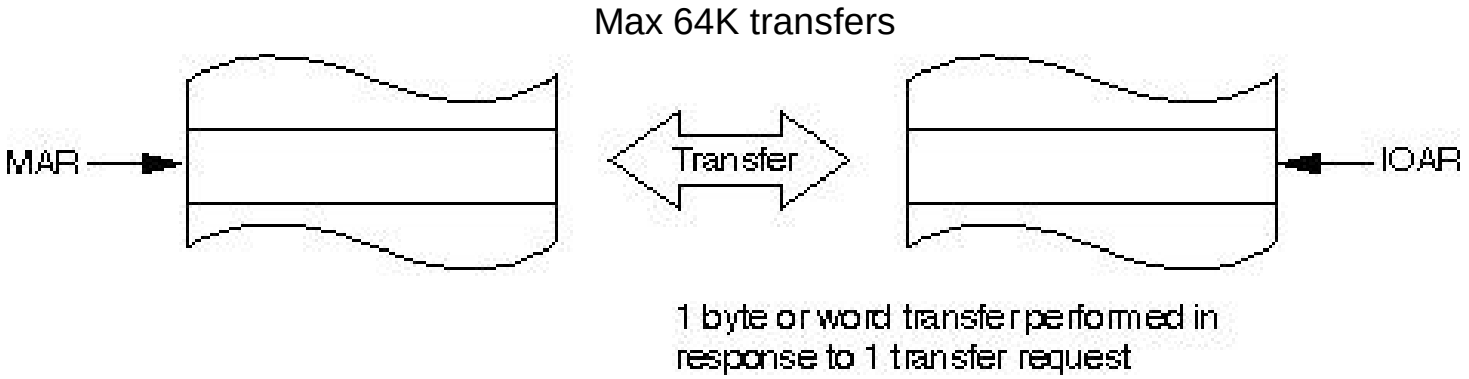


DMAC Sequential (I/O) Operation

H8S/2655 example

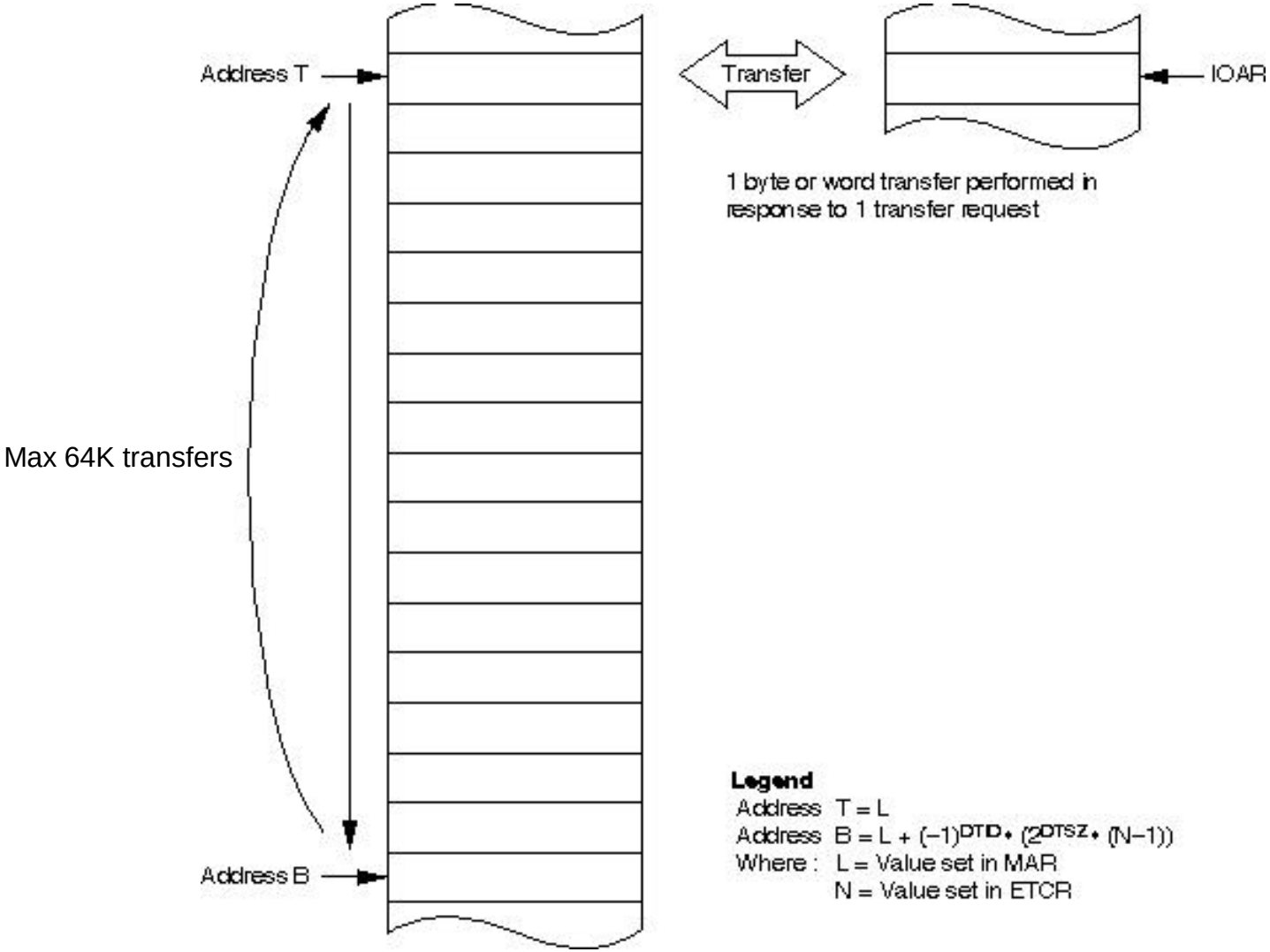


DMAC Idle Operation
H8S/2655 example



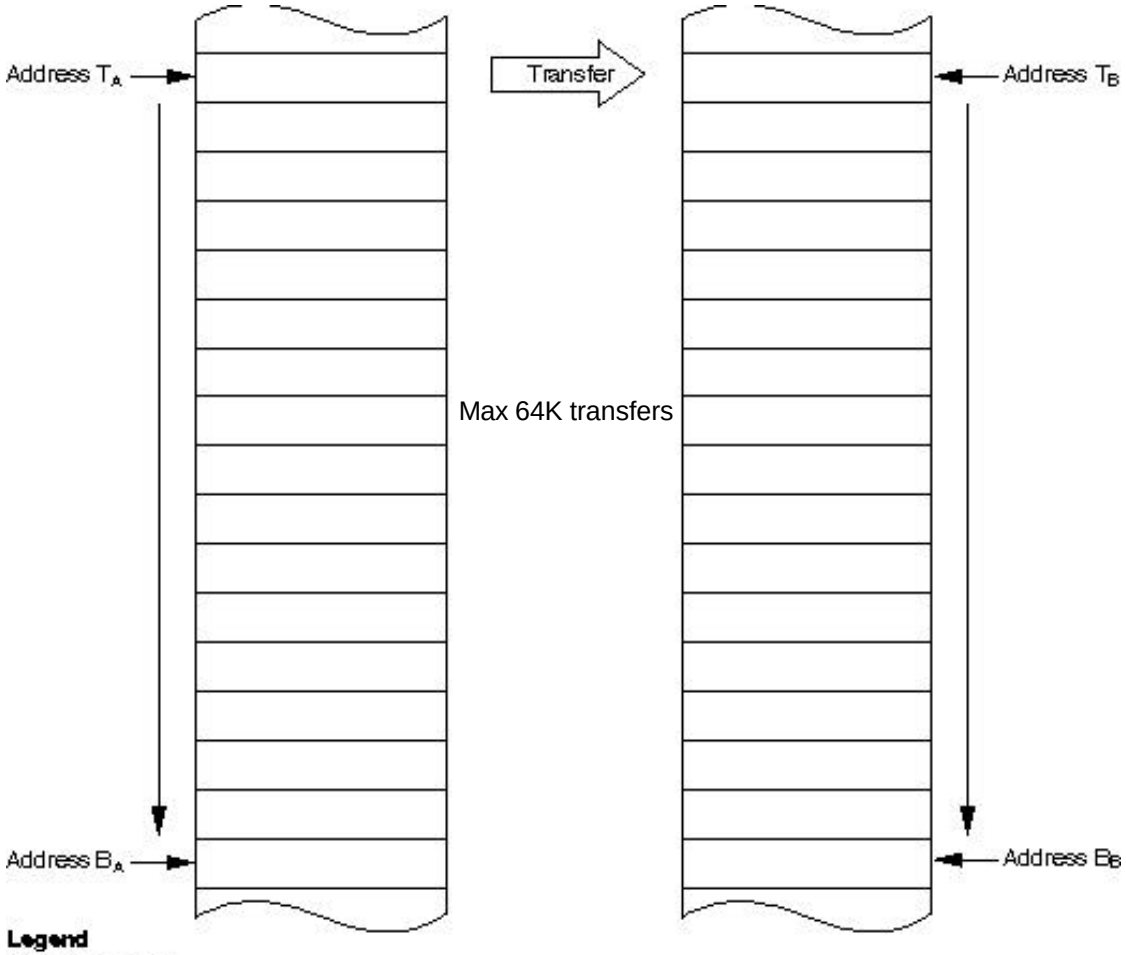
DMAC Repeat Operation

H8S/2655 example



DMAC Normal Mode Operation

H8S/2655 example



Legend

Address $T_A = L_A$

Address $T_B = L_B$

Address $B_A = L_A + SAIDE \cdot (-1)^{SAID} \cdot (2^{DTSZ} \cdot (N-1))$

Address $B_B = L_B + DAIDE \cdot (-1)^{DAID} \cdot (2^{DTSZ} \cdot (N-1))$

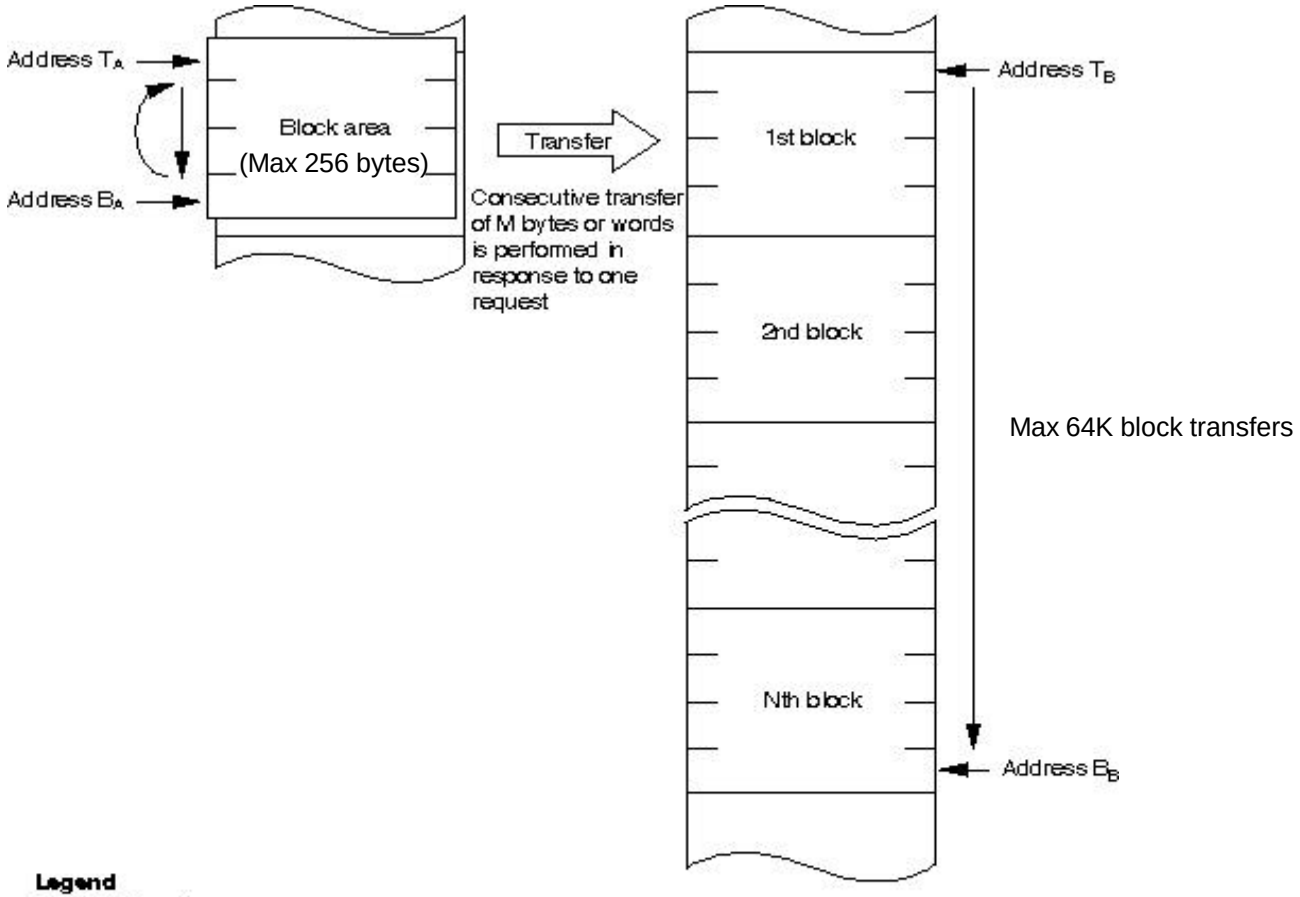
Where : L_A = Value set in MARA

L_B = Value set in MARB

N = Value set in ETCRA

DMAC Block Transfer Operation

H8S/2655 example



Legend

Address $T_A = L_A$
Address $T_B = L_B$
Address $B_A = L_A + SAIDE \cdot (-1)^{SAID} \cdot (2^{DTSZ} \cdot (N-1))$
Address $B_B = L_B + DAIDE \cdot (-1)^{DAID} \cdot (2^{DTSZ} \cdot (M \cdot N-1))$
Where : L_A = Value set in MARA
L_B = Value set in MARB
N = Value set in ETCRB
M = Value set in ETCRAH and ETCRAL

Data Transfer Controller (DTC)
H8S only

Provides DMA-type software-controlled function

Control register information stored in on-chip RAM

Operation features

- One channel transfer at a time
- Transfer possible upon any peripheral interrupt request
- Multiple data transfers can be requested by one activation source

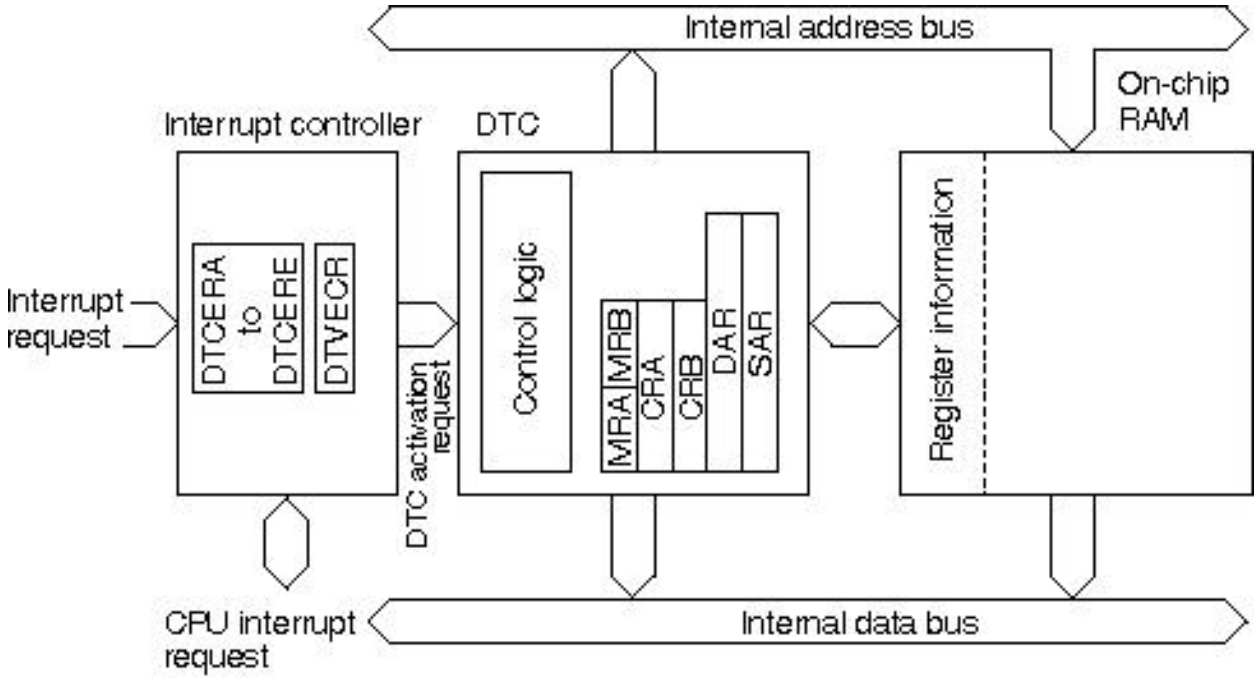
Operation modes

- Normal mode - up to 64K byte/word transfers
- Repeat mode - up to 256 repeat byte/word transfers
- Block transfer mode - up to 64K transfers of max. 256 byte block

Can generate interrupt requests upon transfer completion

DTC Block Diagram

H8S/2148 example



Legend:
MRA, MRB: DTC mode registers A and B
CRA, CRB: DTC transfer count registers A and B
SAR: DTC source address register
DAR: DTC destination address register
DTCERA to DTCERE: DTC enable registers A to E
DTVECR: DTC vector register

Serial Communication Interface (SCI)

Max. 3 channels - IrDA v1.0 support on 1 channel (H8S/21xx)

Asynchronous operation

- Adheres to standard asynchronous communication formats
- Error-checking and break detection capabilities
- Max. 625Kbits/sec.

Synchronous operation

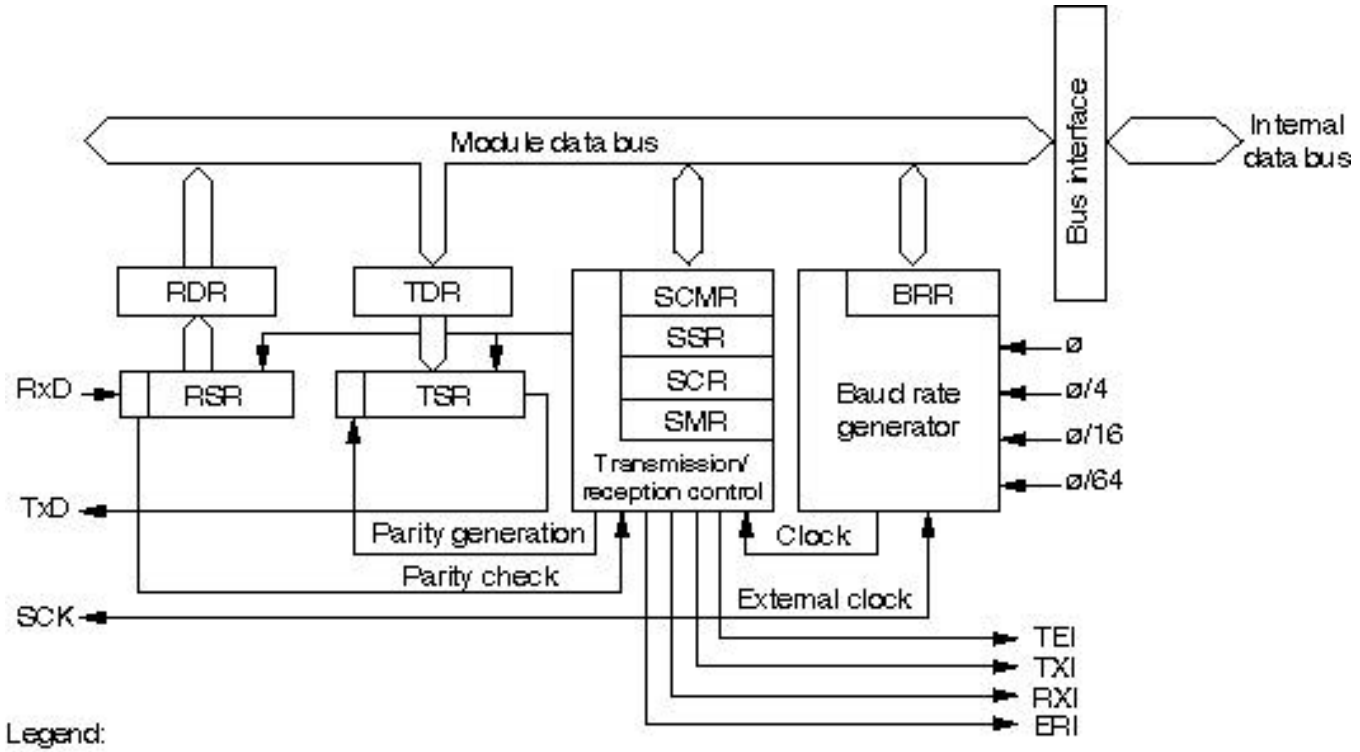
- 8-bit data length
- Max. 4Mbits/sec.

Other features

- Full duplex communication
- Built-in baud rate generator - selectable bit rates
- Selectable clock sources - internal or external
- Interrupts upon end of transmission/receive and/or communication error
- Multiprocessor function - serial communication with multiple devices

SCI Block Diagram

H8S/2144 - one channel example



Legend:

RSR:	Receive shift register
RDR:	Receive data register
TSR:	Transmit shift register
TDR:	Transmit data register
SMR:	Serial mode register
SCR:	Serial control register
SSR:	Serial status register
SCMR:	Serial interface mode register
BRR:	Bit rate register
KBCOMP:	Keyboard comparator control register (for SCI2 IrDA communication)

Smartcard Interface Operation

Only on some H8/300H and H8S/22xx-26xx devices

Uses one SCI channel only

ISO/IEC 7816-3 compliant

Asynchronous communication type

- Supports direct and inverse convention
- Automatic data retransmission
- Error signal detection

Interrupt generating capability

- Transmit buffer empty, receive buffer full

I^2C Interface (H8S/21xx only)

Subset of the Philips I^2C serial bus interface protocol

- Up to 2 channels of 2-wire serial link between H8 and external devices
- Comprises a single data line and a clock line
  - can provide direct bus drive (NMOS open-drain outputs)

Operation features

- Master and slave receive and transmit mode support
- Automatic generation of start/stop conditions
- Wait state insertion during master or slave mode
- Arbitration lost condition identification
- Addressing or non-addressing format support

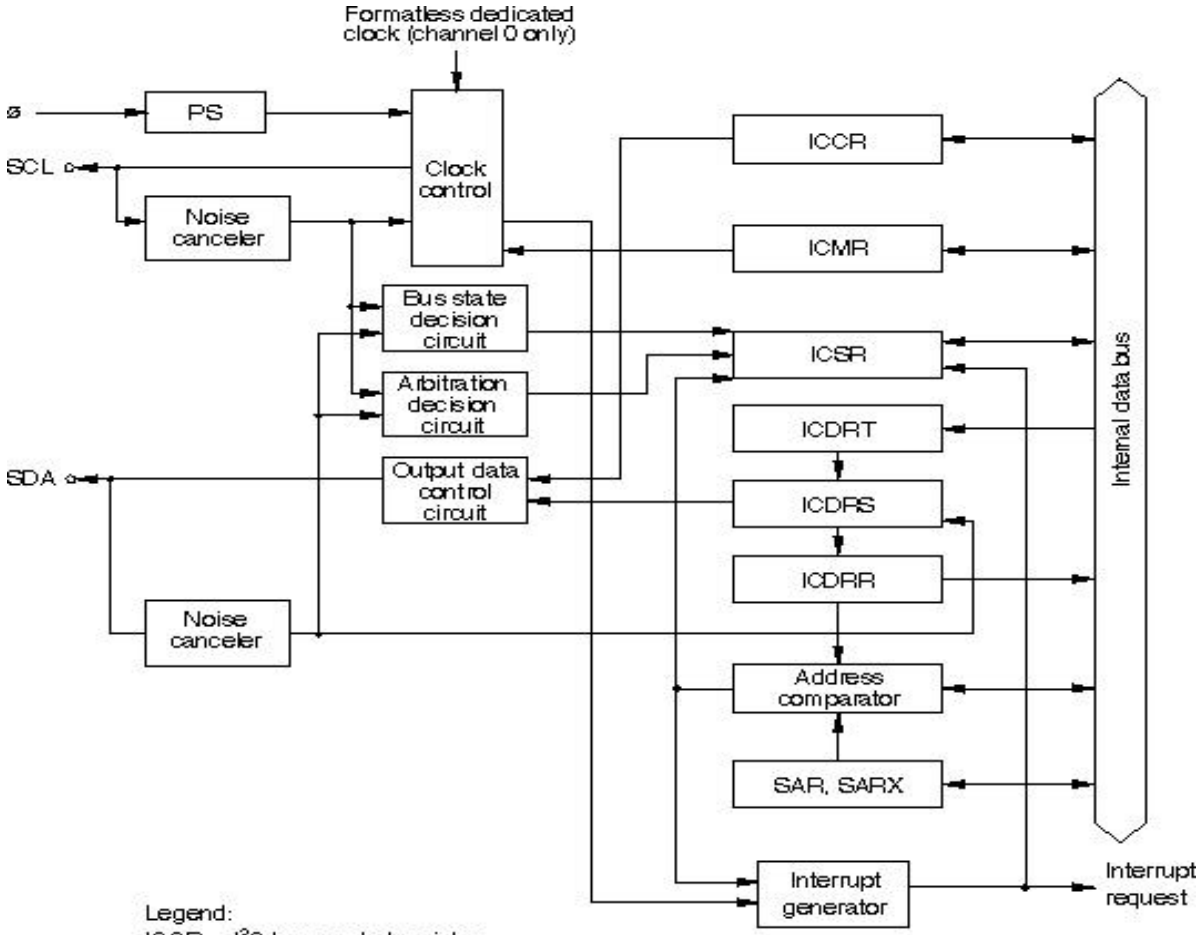
Selection of 16 internal clock sources (master mode)

Three interrupt sources

- Upon data transfer end
- Upon slave address match (in slave receive mode)
- Upon stop condition detection

I²C Interface Block Diagram

H8S/2144 example



Legend:
ICCR: I²C bus control register
ICMR: I²C bus mode register
ICSR: I²C bus status register
ICDR: I²C bus data register
SAR: Slave address register
SARX: Slave address register X
PS: Prescaler

A/D Converter

Up to 8 separate input channels with 10-bit resolution

Up to 2 conversion modes

- Single mode: one channel A/D conversion
- Scan mode: up to 4 channel sequential conversion

Sample-and-hold (S&H) circuit

- 2 interleaved S&H circuits on H8S/2655

Conversion time

- Min. 6.7µs **(most devices)**
- Min. 2.2µs per channel; 1µs continuous conversion **(H8S/2655)**

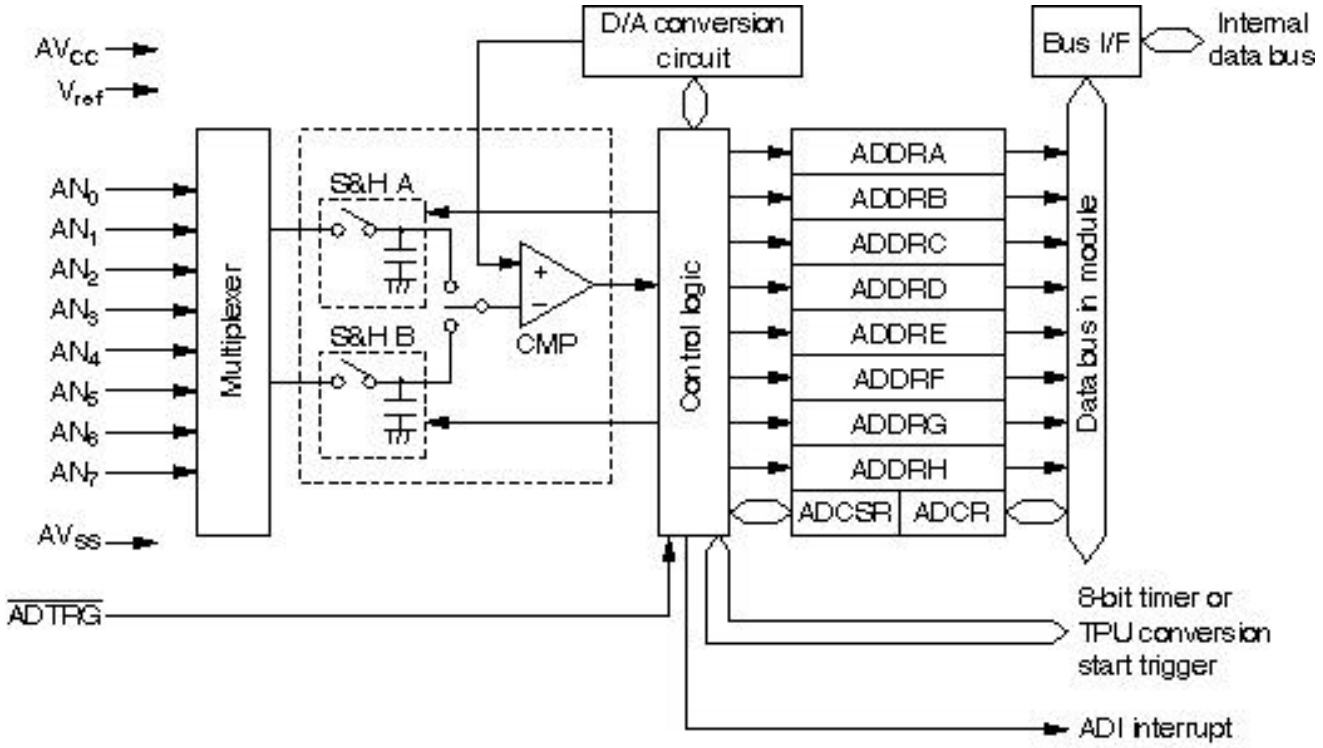
Triggering by s/w, TPU/ 8-bit timer, or by dedicated input pin

Interrupt generating capability upon end of conversion

Selectable analog conversion voltage range

A/D Converter Block Diagram

H8S/2655 example



ADCR : A/D control register
ADCSR : A/D control status register
ADDRA : A/D data register A
ADDRB : A/D data register B
ADDRC : A/D data register C
ADDRD : A/D data register D

CMP : Comparator array
S&H : Sample and hold circuit
ADDRE : A/D data register E
ADDRF : A/D data register F
ADDRG : A/D data register G
ADDRH : A/D data register H

D/A Converter

- Two independent channels
- 8-bit resolution
- Conversion time - max 10ms
- Selectable output voltage range
- D/A output held in software standby mode

Interrupt Processing

Up to 8 priority levels (3 levels for the H8/300H)

Eight level masking

- Decides acceptance of priority interrupts

Independent vector addresses assigned

- No interrupt-identifying handler

External interrupts

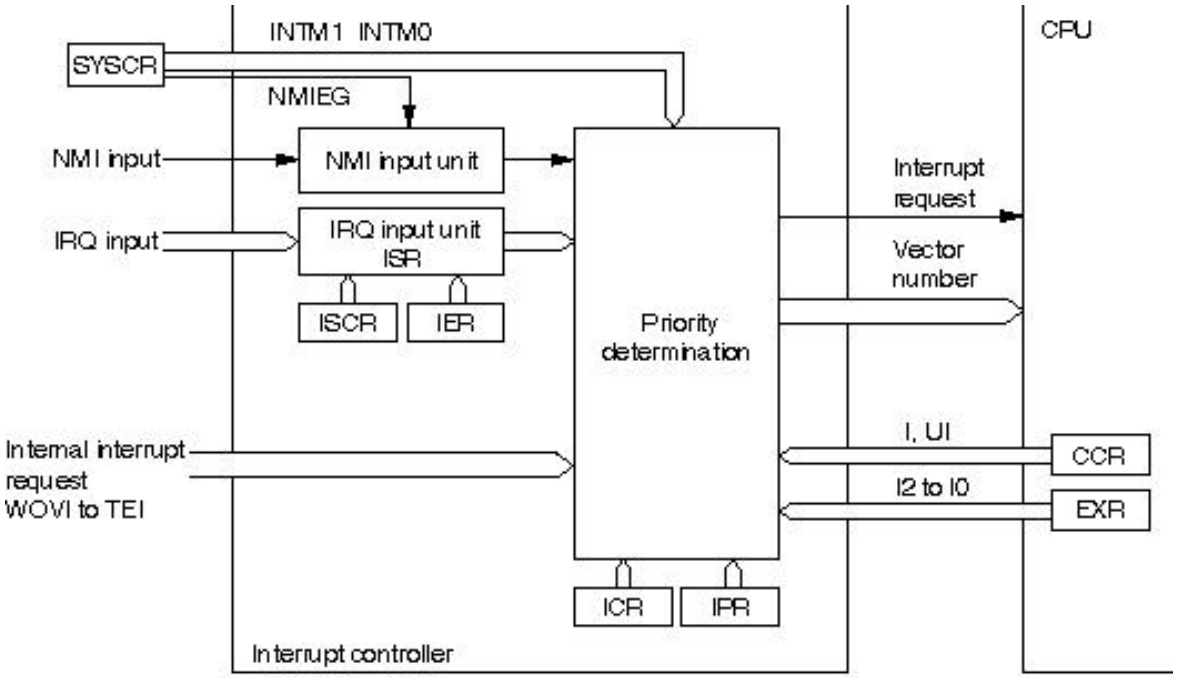
- Max. 9 maskable (IRQs) and 1 non-maskable (NMI)
- NMI triggered upon rising or falling edge
- IRQs triggered upon falling edge, rising edge, or active level

Internal interrupts

- From on-chip peripherals (timers, SCI, A/D, DMAC, refresh ctrl.)

Interrupt Controller Block Diagram

H8S/2655 example



Legend

ISCR	: IRQ sense control register
IER	: IRQ enable register
ISR	: IRQ status register
IPR	: Interrupt priority register
ICR	: Interrupt control register
SYSCR	: System control register