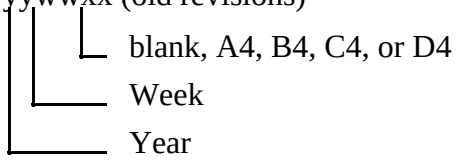
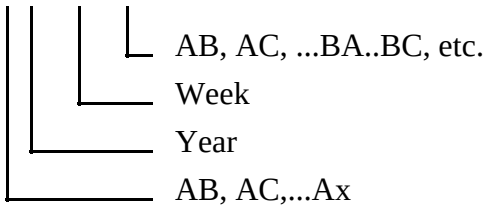
Summary of Differences Between SX18/20/28AC Revisions

Datecode: yywwxx (old revisions)



Datecode:Axyywwxx



Date: 6/7/99

Summary of Changes Between SX18/20/28AC Revisions

	SX18/20/28AC Devices with Datecode yywwxx (old rev)	SX18/20/28AC devices with Datecode Axyywwxx (new rev)
FUSE Word Register (See Note below)	DIV2:DIV0 - Internal RC Oscillator Divider: Bits DIV0, DIV1, and DIV2 are located in bit locations 4, 5, and 6 respectively and provides a selection of 8 frequencies $\overline{\text{OPTIONX}}$ - OPTION Register Extension: Ability to disable programmability of bits 6 and 7 (RTW, RTE_IE bits). STACKX - Stack Extension: Limits the stack size to two levels or extends the size to 8 levels.	DIV1:DIV0 - Internal RC Oscillator Divider: Bits DIV0, and DIV1 are located in bit locations 5, and 6 respectively and provides a selection of 4 frequencies. Bit 4 is reserved.Bit DIV0 and DIV1 also dual functions. DIV0 (FOSC2) extends the external oscillator configuration. DIV1 ($\overline{\text{IFBD}}$) is the internal feedback resistor disable bit for the external resonator/crystal oscillator. Moved to bit 7 of the FUSEX register. The bit position is reserved. Moved to bit 7 of the FUSEX register. The bit position is reserved.
FUSEX Word Register (See Note below)	MEM1:MEM0 - Configure Program Memory Size: Configures the program memory size if desired to be different than the factory setting. RAM1:RAM0 - Configure Number of RAM Banks: Configures the number of RAM banks if desired to be different than the factory setting. BOR1:BOR0 - Brown-Out Reset: Can disable the Brown-Out feature or enable and set the trip point to 4.2V.	BP1:BP0 - These bits configure both the program memory size and the number of RAM banks. See the register map for details. The bit locations are used for trimming the Brown-Out trip point (factory untrimmed). The number of RAM banks is selected through the BP1 and BP0 bits. BOR1:BOR0 - Brown-Out Reset: Can disable Brown -Out feature or enable and select 3 different trip points.
External Crystal/Resonator (LP, XT, or HS Mode)	The FOSC1:FOSC0 bits provide 3 settings.	The FOSC2:FOSC0 bits provide 7 settings.
External Crystal/Resonator Oscillator Component Values	Specified in the datasheet (latest version is dated 2/11/99)	The component values (Rf, C1, C2) values are different. Target values are available for reference.
Supply Voltage	4.5V to 6.25V	2.5V to 5.5V
Parallel/Serial Prog. Times	100 ms/word	< 20 ms/word
Tools Support	SX Key Rev E, Soft Rev 1.05	SX Key Rev E, Soft Rev 1.06 or higher

Note: The development tools are updated to make the impact of changes transparent to the user.

Device Configuration Options

The register formats are shown in Figure 1 and the configuration fields within the registers are explained in Table 2 through Table 5. Note that the register formats vary, depending on the SX datecode variations. .

FUSE Word for SX18/20/28AC Devices with Datecode yywwxx (old revisions)

$\overline{\text{TURBO}}$	$\overline{\text{SYNC}}$	$\overline{\text{OPTIONX}}$	$\overline{\text{STACKX}}$	$\overline{\text{IRC}}$	DIV2	DIV1	DIV0	$\overline{\text{CP}}$	WDTE	FOSC1	FOSC0
Bit 11											**Bit 0**

FUSE Word for SX18/20/28AC Devices with Datecode Axyywwxx (new revision)

$\overline{\text{TURBO}}$	$\overline{\text{SYNC}}$	Reserved	Reserved	$\overline{\text{IRC}}$	DIV1/ $\overline{\text{IFBD}}$	DIV0/ FOSC2	Reserved	$\overline{\text{CP}}$	WDTE	FOSC1	FOSC0
Bit 11											**Bit 0**

FUSEX Word for SX18/20/28AC Devices with Datecode yywwxx (old revisions)

IRCTRIM2	PINS	IRCTRIM1	IRCTRIM0	Reserved	$\overline{\text{CF}}$	BOR1	BOR0	RAM1	RAM0	MEM1	MEM0
Bit 11											**Bit 0**

FUSEX Word for SX18/20/28AC Devices with Datecode Axyywwxx (new revision)

IRCTRIM2	PINS	IRCTRIM1	IRCTRIM0	$\overline{\text{OPTIONX}}$/ $\overline{\text{STACKX}}$	$\overline{\text{CF}}$	BOR1	BOR0	BORTRIM1	BORTRIM0	BP1	BP0
Bit 11											**Bit 0**

Figure 1 Device Configuration Register Formats

External Crystal/Resonator (XT, LP, or HS Mode)

SX18/20/28AC devices with datecode Axyywwxx (new revision) support extended crystal/resonator modes. Table 3 shows the different mode being supported. The new version of the device has improved internal crystal/resonator support circuitry. The external component values associated with oscillator circuit may have to chnage when using the new version. The oscillator circuit is currently being characterized. Contact Scenix for the component values.

Table 2 FUSE Word Bits for SX18/20/28AC with Datecode yywwxx (old revisions)

Option Bits	Description
$\overline{\text{TURBO}}$	Turbo Mode. Set to 1 for “compatible” mode, in which the instruction rate operates at one-fourth the oscillator clock rate. Set to 0 for the turbo mode, in which the instruction rate is equal to the oscillator clock rate.
$\overline{\text{SYNC}}$	Synchronous Input Mode (for turbo mode operation). Set to 1 to disable or clear to 0 to enable synchronous inputs.
$\overline{\text{OPTIONX}}$	OPTION Register Extension. Set to 1 to disable the programmability of bit 6 and bit 7 in the OPTION register, the RTW and RTE_IE bits (in other words, to force these two bits to 1). Clear to 0 to enable programming of the RTW and RTE_IE bits in the OPTION register.
$\overline{\text{STACKX}}$	Stack Extension. Set to 1 to limit the stack size to two locations. Clear to 0 to extend the stack size to eight locations.
$\overline{\text{IRC}}$	Internal RC Oscillator. Set to 1 to disable the internal oscillator and have the OSC1 and OSC2 pins operate as defined by the FOSC1:FOSC0 bits. Clear to 0 to enable the internal oscillator, and to have the OSC1 pin floating and the OSC2 pin weakly pulled high.
DIV2:DIV0	Internal RC Oscillator Divider. This field sets the divide-by factor for generating the instruction clock from the internal oscillator when the internal oscillator is enabled ($\overline{\text{IRC}}$ = 0). The nominal instruction rate is determined by DIV2:DIV0 as follows: 000 = 4 MHz 001 = 2 MHz 010 = 1 MHz 011 = 500 kHz 100 = 250 kHz 101 = 125 kHz 110 = 62.5 kHz 111 = 31.25 kHz
$\overline{\text{CP}}$	Code Protection. Set to 1 for no code protection. Clear to 0 for code protection. With code protection, the program code and configuration registers read back as scrambled data. This prevents reverse-engineering of your proprietary code and configuration options.
WDTE	Watchdog timer enable. Set to 1 to enable the Watchdog timer. Clear to 0 to disable the Watchdog timer.
FOSC1: FOSC0	External Oscillator Configuration. This field sets up the device to operate with a particular type of external oscillator when the device is configured to operate with an external oscillator ($\overline{\text{IRC}}$ = 1). The type of external oscillator is determined by FOSC1:FOSC0 as follows: 00 = LP – low-power crystal 01 = XT – normal crystal 10 = HS – high-speed crystal 11 = RC network – OSC2 is weakly pulled high and no CLKOUT output

Table 3 FUSE Word Bits for SX18/20/28AC with Datecode Axyywwxx (new revision)

Option Bits	Description
$\overline{\text{TURBO}}$	Turbo Mode. Set to 1 for “compatible” mode, in which the instruction rate operates at one-fourth the oscillator clock rate. Set to 0 for the turbo mode, in which the instruction rate is equal to the oscillator clock rate.
$\overline{\text{SYNC}}$	Synchronous Input Mode (for turbo mode operation). Set to 1 to disable or clear to 0 to enable synchronous inputs.
$\overline{\text{IRC}}$	Internal RC Oscillator. Set to 1 to disable the internal oscillator and have the OSC1 and OSC2 pins operate as defined by the FOSC1:FOSC0 bits. Clear to 0 to enable the internal oscillator, and to have the OSC1 pin floating and the OSC2 pin weakly pulled high.
DIV1:DIV0	Internal RC Oscillator Divider. This field sets the divide-by factor for generating the instruction clock from the internal oscillator when the internal oscillator is enabled ($\overline{\text{IRC}}$ = 0). The nominal instruction rate is determined by DIV1:DIV0 as follows: 00 = 4 MHz 01 = 1 MHz 10 = 128 kHz 11 = 32 kHz
$\overline{\text{IFBD}}$	Internal Feedback Disable. If $\overline{\text{IRC}}$ = 1, and $\overline{\text{IFBD}}$ = 1, the crystal/resonator oscillator can rely on the internal feedback resistor between the OSC1 and OSC2 pins. If IFBD = 0, an external feedback resistor is required between the OSC1 and OSC2 pins.
$\overline{\text{CP}}$	Code Protection. Set to 1 for no code protection. Clear to 0 for code protection. With code protection, the program code and configuration registers read back as scrambled data. This prevents reverse-engineering of your proprietary code and configuration options.
WDTE	Watchdog timer enable. Set to 1 to enable the Watchdog timer. Clear to 0 to disable the Watchdog timer.
FOSC2: FOSC0	External Oscillator Configuration. This combination of three register bits sets up the device to operate with a particular type of external oscillator when the device is configured to operate with an external oscillator ($\overline{\text{IRC}}$ = 1). Note that bit 5, the DIV0/FOSC2 bit, operates as DIV0 with $\overline{\text{IRC}}$=0, or as FOSC2 with $\overline{\text{IRC}}$=1. The type of external oscillator is determined by FOSC2:FOSC0 as follows: 000 = LP1 – low-power crystal (32 KHz) 001 = LP2 – low-power crystal (32 KHz to 1 MHz) 010 = XT1 – normal crystal (32 KHz to 10 MHz) 011 = XT2 – normal crystal (1 MHz to 24 MHz) 100 = HS – high speed crystal (1 MHZ to 50 MHz) 101 = Reserved 110 = Reserved 111 = External RC Note: The frequency ranges have not been characterized. These are target values.

Table 4 FUSEX Bits for SX18/20/28AC with Datecode yywwxx (old revisions)

Option Bits	Description
IRCTRIM2: IRCTRIM0	Internal RC Oscillator Trim. This 3-bit field adjusts the operation of the internal RC oscillator to make it operate within the target frequency range of 4.0 MHz plus or minus 8%. Parts are shipped from the factory untrimmed. The device relies on the programming tool to provide the trimming function.
$\overline{CF}$	Carry Flag Input. Set to 1 to ignore the carry flag as an input to addition and subtraction operations. Clear to 0 to add the carry flag into all addition operations (ADD fr,W means fr = fr + W + C); and to subtract the complement of the carry flag from all subtraction operations (SUB fr,W means fr = fr – W – /C).
BOR1: BOR0	Brown-Out Reset. These two factory-configured bits should not be changed unless you want to enable the brown-out functionality of the device. To enable the brown-out feature (4.2V trip level), set these bits to 01. To disable the brown-out feature set both bits to 1.
RAM1: RAM0	Configured Number of RAM Banks. These two factory-configured bits should not be changed unless you want to reduce the configured amount of RAM in the device. To do so, use one the following RAM1:RAM0 settings: 00 = 1 bank 01 = 2 banks 10 = 4 banks 11 = 8 banks (default)
MEM1: MEM0	Configured Memory Size. These two factory-configured bits should not be changed unless you want to reduce the configured amount of program memory in the device. To do so, use one the following MEM1:MEM0 settings: 00 = 1 page 01 = 1 page 10 = 4 pages 11 = 8 pages (default)

Table 5 FUSEX Bits for SX18/20/28AC with Datecode Axyywwxx (new revision)

Option Bits	Description
IRCTRIM2: IRCTRIM0	Internal RC Oscillator Trim. This 3-bit field adjusts the operation of the internal RC oscillator to make it operate within the target frequency range of 4.0 MHz plus or minus 8%. Parts are shipped from the factory untrimmed. The device relies on the programming tool to provide the trimming function.
$\overline{\text{OPTIONX}}$/ $\overline{\text{STACKX}}$	OPTION Register Extension and Stack Extension. Set to 1 to disable the programmability of bit 6 and bit 7 in the OPTION register, the RTW and RTE_IE bits (in other words, to force these two bits to 1); and to limit the program stack size to two locations. Clear to 0 to enable programming of the RTW and RTE_IE bits in the OPTION register, and to extend the stack size to eight locations.
$\overline{\text{CF}}$	Carry Flag Input. Set to 1 to ignore the carry flag as an input to addition and subtraction operations. Clear to 0 to add the carry flag into all addition operations (ADD fr,W means fr = fr + W + C); and to subtract the complement of the carry flag from all subtraction operations (SUB fr,W means fr = fr – W – /C).
BOR1: BOR0	Brown-Out Reset. The BOR1:BOR0 bits enable or disable the brown-out reset function and set the brown-out threshold voltage as follows: 00 = 4.2V 01 = 2.6V 10 = 2.2V 11 = Disable Brown-Out Reset
BORTRIM1: BORTRIM0	Brown-Out trim bits (parts are shipped out of the factory untrimmed).
BP1: BP0	Configured Memory Size. These two factory-configured bits should not be changed unless you want to reduce the configured amount of program memory in the device. To do so, use one the following BP1:BP0 settings: 00 = 1 page, 1 bank 01 = 1 page, 2 banks 10 = 4 pages, 4 banks 11 = 4 pages, 8 banks (default)

DC Electrical Characteristics (Target Specs)

SX18AC/SX20AC/SX28AC (Datecode Axyywwxx, new revision); Operating Temperature 0° C <= Ta <= +70° C (Commercial)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{dd}	Supply Voltage		2.5	-	5.5	V
V_{por}	V_{dd} start voltage to ensure Power-On Reset		V_{ss}	-	-	V
S_{Vdd}	V_{dd} rise rate		0.05	-	-	V/ms
I_{dd}	Supply Current, active	V_{dd} = 5.0V, F_{osc} = 50 MHz V_{dd} = 5.0V, F_{osc} = 4 MHz internal V_{dd} = 2.5V, F_{osc} = 20 MHz	-	65 6 12	-	mA mA mA
I_{pd}	Supply Current, power down	V_{dd} = 5.5V, WDT enabled V_{dd} = 5.5V, WDT disabled V_{dd} = 2.5V, WDT enabled V_{dd} = 2.5V, WDT disabled	-	TBD 1.0 TBD 500	-	µA µA µA nA
V_{ih}, V_{il}	Input Levels $\overline{MCLR}$, OSC1, RTCC Logic High Logic Low All Other Inputs CMOS Logic High Logic Low TTL Logic High Logic Low		 0.8V_{dd} V_{ss} 0.7V_{dd} V_{ss} 2.0 V_{ss}		 V_{dd} 0.2V_{dd} V_{dd} 0.3V_{dd} V_{dd} 0.8	 V V V V V V
I_{il}	Input Leakage Current	V_{in} = V_{dd} or V_{ss}	-1.0		+1.0	µA
I_{ip}	Weak Pullup Current	V_{dd} = 5.0V, V_{in} = 0V V_{dd} = 2.5V, V_{in} = 0V			400 80	µA µA
V_{oh}	Output High Voltage OSC2, Ports B, C Port A	 Ioh = 20mA, Vdd = 4.5V Ioh = 12mA, Vdd = 2.5V Ioh = 30mA, Vdd = 4.5 Ioh = 18 mA, Vdd = 2.5V	 Vdd-0.7 Vdd-0.7 Vdd-0.7 Vdd-0.7			 V V V V
V_{ol}	Output Low Voltage All Ports, OSC2	Iol = 30mA, Vdd = 4.5V Iol = 18mA, Vdd = 2.5V			0.6 0.6	V V

AC Electrical Characteristics (Target Specs)

SX18AC/20AC/28AC (Datecode Axyywwxx, new revision); Operating Temperature 0° C <= Ta <= +70° C (Commercial)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
F_{osc}	External CLKIN Frequency	DC	-	4.0	MHz	RC
				10	MHz	XT1
				24	MHz	XT2
				50	MHz	HS
				32	KHz	LP1
				1.0	MHz	LP2
	Oscillator Frequency	DC	-	4.0	MHz	RC
		0.032		10.0	MHz	XT1
		1.0		24.0	MHz	XT2
		1.0		50	MHz	HS
		DC		32	KHz	LP1
		0.032		1.0	MHz	LP2
T_{osc}	External CLKIN Period	250	-	-	ns	RC
		100			ns	XT1
		41.7			ns	XT2
		20			ns	HS
		31.25			µs	LP1
		1.0			µs	LP2
	Oscillator Period	250	-	-	ns	RC
		100		31.25	µs	XT1
		41.7		1.0	µs	XT2
		20		1.0	µs	HS
		31.25		-	µs	LP1
		1.0		31.25	µs	LP2
T_{osL}, T_{osH}	Clock in (OSC1) Low or High Time	50	-	-	ns	XT1/XT2
		8.0			ns	HS
		2.0			µs	LP1/LP2
T_{osR}, T_{osF}	Clock in (OSC1) Rise or Fall Time	-	-	25	ns	XT1/XT2
				25	ns	HS
				50	µs	LP1/LP2

Note: Data in the Typical ("TYP") column is at 5V, 25° C unless otherwise stated.

Internal RC Oscillator AC specs are still being characterized. Specification is 4MHz ± 8% over commercial temp (0° C- 70° C) range.

Comparator DC and AC Specifications (Target Specs)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage	0.4V < Vin < Vdd – 1.5V		+/- 10	+/- 25	mV
Input Common Mode Voltage Range		0.4		Vcc – 1.3	V
Voltage Gain			300k		V/V
DC Supply Current (enabled)	Vdd = 5.5V			120	µA
Response Time	$V_{overdrive}$ = 25mV			250	ns